

# **BUK761R6-40E**

# N-channel TrenchMOS standard level FET 5 September 2013

**Product data sheet** 

#### **General description** 1.

Standard level N-channel MOSFET in a SOT404A package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

#### **Features and benefits** 2.

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with V<sub>GS(th)</sub> rating of greater than 1 V at 175 °C

### **Applications**

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

#### Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	40	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	[1]	-	-	120	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	349	W
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 11		_	1.3	1.57	mΩ
Dynamic characteristics							
$Q_{GD}$	gate-drain charge	$V_{GS}$ = 10 V; $I_D$ = 25 A; $V_{DS}$ = 32 V; Fig. 13; Fig. 14		-	48.2	-	nC

[1] Continuous current is limited by package.



# 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D I
2	D	drain		
3	S	source		G T T
mb	D	mounting base; connected to drain	D2PAK (SOT404A)	mbb076 S

# 6. Ordering information

Table 3. Ordering information

Type number	Package						
	Name	Description	Version				
BUK761R6-40E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404A				

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK761R6-40E	BUK761R6-40E

# 8. Limiting values

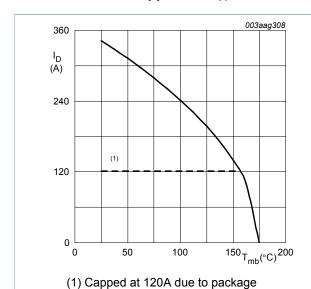
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS}$ = 20 k $\Omega$		-	40	V
V <sub>GS</sub>	gate-source voltage	T <sub>j</sub> ≤ 175 °C; DC		-20	20	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; <u>Fig. 1</u>	[1]	-	120	Α
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 10 V; <u>Fig. 1</u>	[1]	-	120	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; Fig. 4		-	1355	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	349	W
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
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Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	120	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	1355	Α
Avalanche	ruggedness		1			
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 120 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[2][3]	-	1008	mJ

- Continuous current is limited by package. Single-pulse avalanche rating limited by maximum junction temperature of 175  $^{\circ}\text{C}.$
- Refer to application note AN10273 for further information.



Continuous drain current as a function of Fig. 1. mounting base temperature

 $V_{GS} \ge 10V$ 

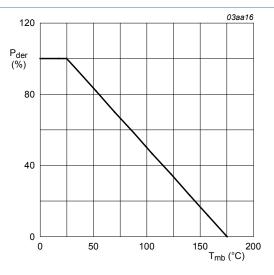


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

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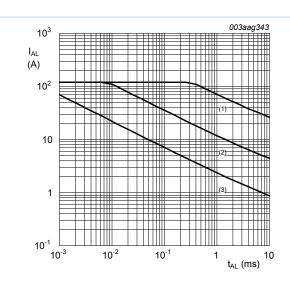
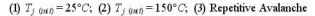


Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



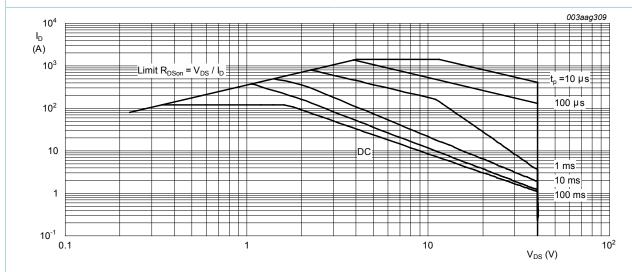


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

#### 9. Thermal characteristics

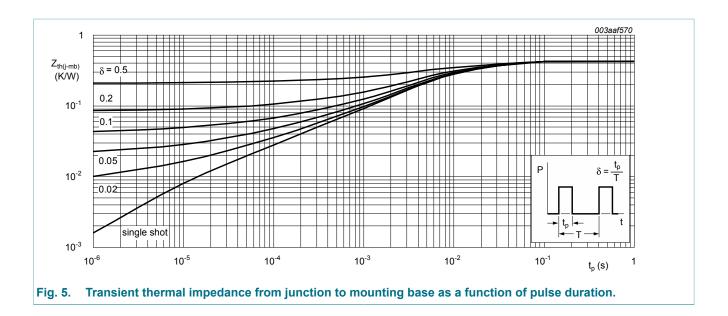
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	-	0.43	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

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### 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
(5.1)500	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	40	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 10	-	-	4.5	V
	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 10	1	-	-	V	
I <sub>DSS</sub> drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.25	2	μA	
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μΑ
I <sub>GSS</sub> g	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		$V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; Fig. 11	-	1.3	1.57	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 12; Fig. 11	-	-	3	mΩ
Dynamic ch	naracteristics			'		_
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V;	-	145	-	nC
Q <sub>GS</sub>	gate-source charge	Fig. 13; Fig. 14	-	35.7	-	nC
$Q_{GD}$	gate-drain charge	1	-	48.2	-	nC

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz;		-	8500	11340	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>		-	1620	1950	pF
C <sub>rss</sub>	reverse transfer capacitance			-	985	1350	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_{L} = 1.2 \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5 \Omega$		-	42	-	ns
t <sub>r</sub>	rise time			-	60	-	ns
$t_{d(off)}$	turn-off delay time			-	121	-	ns
t <sub>f</sub>	fall time			-	83	-	ns
L <sub>D</sub>	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nΗ
L <sub>S</sub>	internal source inductance	from source lead to source bonding pad		-	7.5	-	nΗ
Source-dra	in diode				'	'	
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$		-	0.77	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	56	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V		-	94	-	nC

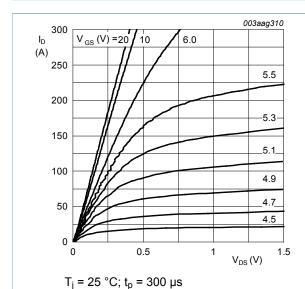


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

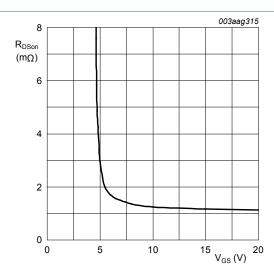


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25 \,^{\circ}C; I_D = 25A$$

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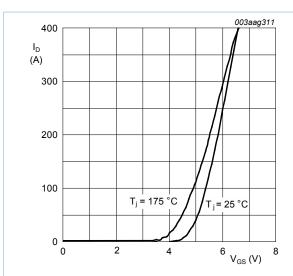


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



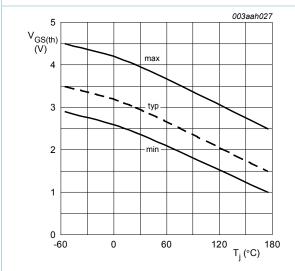


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$

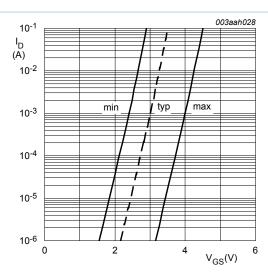
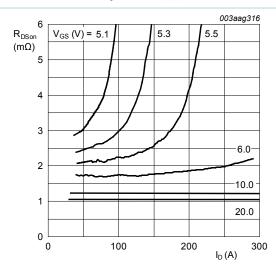


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$



 $T_i = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$ 

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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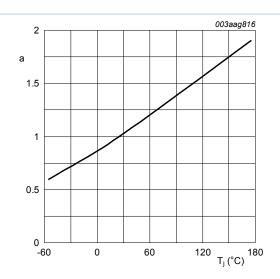
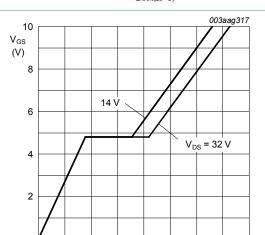


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\mathbf{a} = \frac{R_{DSon}}{R_{DSon(25~\mathrm{C})}}$$



 $T_i = 25 \,^{\circ}\text{C}; I_D = 25 \,\text{A}$ 

40

Fig. 14. Gate-source voltage as a function of gate charge; typical values

 $^{120}_{Q_G(nC)}^{160}$ 

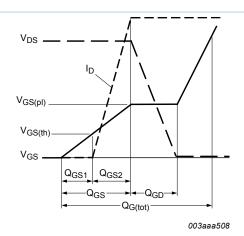


Fig. 13. Gate charge waveform definitions

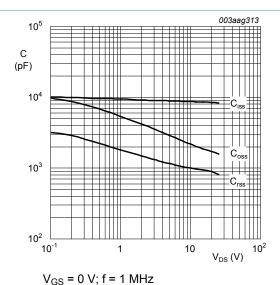
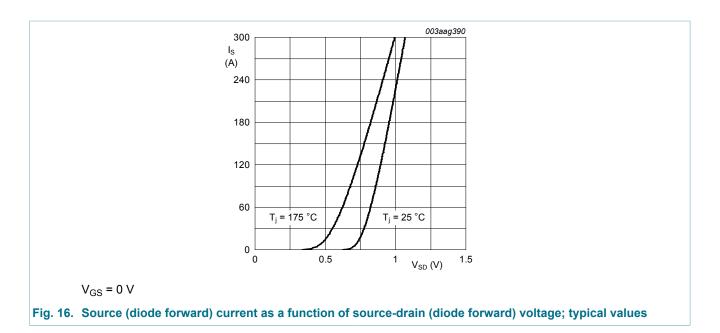
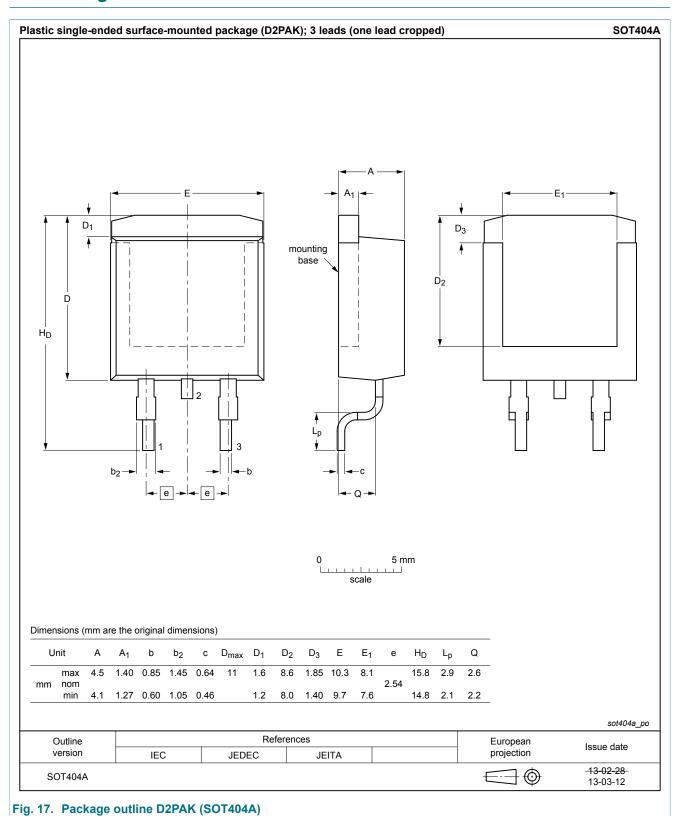


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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# 11. Package outline



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### 12. Legal information

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### 13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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