# NX3DV642

## 3-lane high-speed MIPI compatible switch

Rev. 1 — 20 August 2012 Product data sheet

## 1. General description

The NX3DV642 is a high-speed triple-pole double-throw differential signal switch. The device is optimized for switching between two MIPI devices, such as cameras or LCD displays and on-board multimedia application processors.

The NX3DV642 is compatible with the requirements of Mobile Industry Processor Interface (MIPI). The low capacitance design allows the NX3DV642 to switch signals that exceed 500 MHz in frequency

## 2. Features and benefits

- Supply voltage range from 2.65 V to 4.3 V
- 7.5 Ω typical ON resistance
- 8.4 pF typical ON capacitance
- 950 MHz typical bandwidth or data frequency
- Low crosstalk of −55 dB at 100 MHz
- Break-before-make switching
- ESD protection:
  - HBM JESD22-A114F Class 2 exceeds 2000 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
  - HBM exceeds 12000 V for power to GND protection
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Specified from −40 °C to +85 °C

## 3. Applications

- Dual camera applications for cell phones
- Dual LCD applications for cell phones, digital camera displays and viewfinders

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| NX3DV642GU | −40 °C to +85 °C | XQFN24 | plastic, extremely thin quad flat package; no leads; 24 terminals; body 2.5 x 3.4 x 0.5 mm | SOT1310-1 |

## 5. Marking

**Table 2. Marking**

| Type number | Marking code |
|---|---|
| NX3DV642GU | 3DV642 |

## 6. Functional diagram

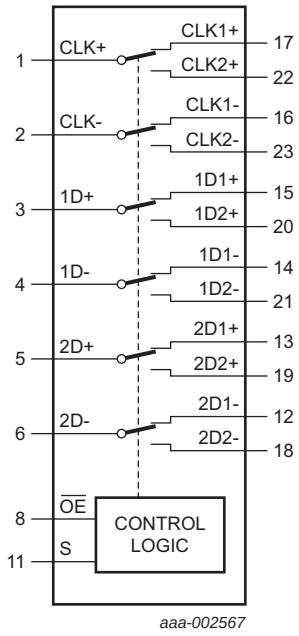



**Fig 1. Logic symbol**

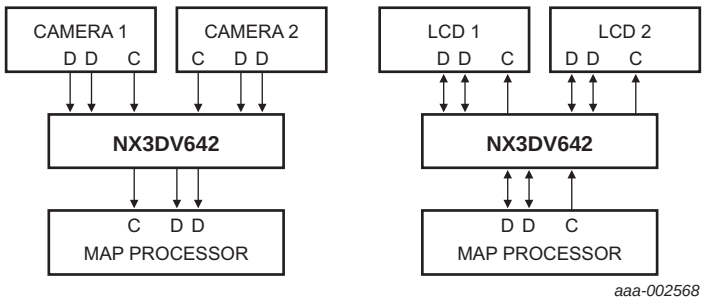



**Fig 2. Application block diagram**

# 7. Pinning information

## 7.1 Pinning

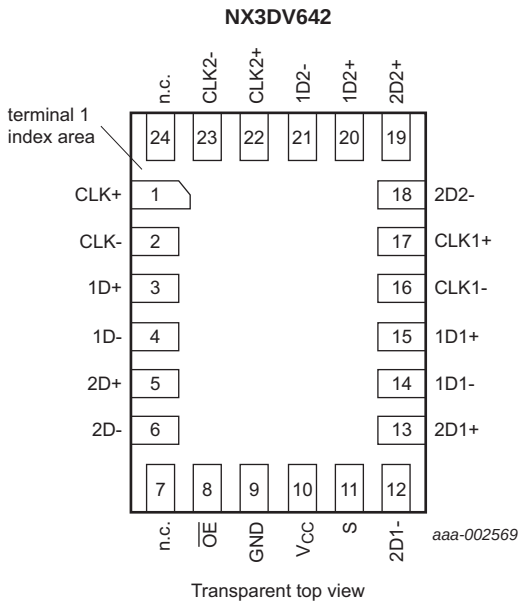



**Fig 3. Pin configuration SOT1310-1 (XQFN24)**

## 7.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| CLK+, CLK– | 1, 2 | common output or input clock path |
| 1D+, 1D– | 3, 4 | common output or input data path 1D |
| 2D+, 2D– | 5, 6 | common output or input data path 2D |
| n.c. | 7, 24 | not connected |
| $\overline{OE}$ | 8 | output enable input (active LOW) |
| GND | 9 | ground (0 V) |
| $V_{CC}$ | 10 | supply voltage |
| S | 11 | select input |
| 2D1+, 2D1– | 13, 12 | independent input or output data path 2D1 |
| 1D1+, 1D1– | 15, 14 | independent input or output data path 1D1 |
| CLK1+, CLK1– | 17, 16 | independent input or output clock path CLK1 |
| 2D2+, 2D2– | 19, 18 | independent input or output data path 2D2 |
| 1D2+, 1D2– | 20, 21 | independent input or output data path 1D2 |
| CLK2+, CLK2– | 22, 23 | independent input or output clock path CLK2 |

# 8. Functional description

**Table 4. Function table[1]**

| Input | | Channel on |
|---|---|---|
| **S** | **$\overline{OE}$** | |
| L | L | CLKn, 1Dn, 2Dn = CLK1n, 1D1n, 2D1n |
| H | L | CLKn, 1Dn, 2Dn = CLK2n, 1D2n, 2D2n |
| X | H | switch off |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care. (n = + or –)

# 9. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +5.5 | V |
| $V_I$ | input voltage | pins S and $\overline{OE}$ | [1] | –0.5 | +5.5 | V |
| $V_{SW}$ | switch voltage | | | –0.5 | +5.5 | V |
| $I_{IK}$ | input clamping current | $V_I$ < –0.5 V | | –50 | - | mA |
| $I_{SK}$ | switch clamping current | $V_I$ < –0.5 V | | –50 | +50 | mA |
| $I_{SW}$ | switch current | | | –100 | +100 | mA |
| $I_{CC}$ | supply current | | | - | +50 | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +85 °C | | - | 533 | mW |

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

# 10. Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | 2.65 | 4.3 | V |
| $V_I$ | input voltage | pins S and $\overline{OE}$ | | 0 | 4.3 | V |
| $V_{SW}$ | switch voltage | | [1] | 0 | 4.5 | V |
| $T_{amb}$ | ambient temperature | | | –40 | +85 | °C |

[1] To avoid sinking GND current from terminals CLKn, 1Dn and 2Dn when switch current flows in terminals CLK1n, CLK2n, 1D1n 1D2n, 2D1n and 2D2n (n = + or –), the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals CLKn, 1Dn and 2Dn, no GND current flows from terminals CLK1n, CLK2n, 1D1n 1D2n, 2D1n and 2D2n. In this case, there is no limit for the voltage drop across the switch.

# 11. Static characteristics

**Table 7. Static characteristics**

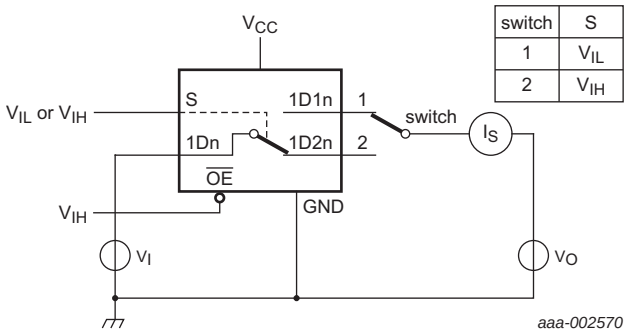
*At recommended operating conditions; voltages are referenced to GND (ground 0 V).*

| Symbol | Parameter | Conditions | | $T_{amb}$ = –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.65 V to 2.775 V | | 1.3 | - | - | V |
| | | $V_{CC}$ = 4.3 V | | 1.7 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.65 V to 2.775 V | | - | - | 0.5 | V |
| | | $V_{CC}$ = 4.3 V | | - | - | 0.7 | V |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 2.775 V; $I_I$ = –18 mA | | –1.2 | - | - | V |
| $I_I$ | input leakage current | pins S and $\overline{OE}$; $V_I$ = GND to 4.3 V; $V_{CC}$ = 4.3 V | | - | - | ±1 | µA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 4.3 V; see Figure 4 | | - | - | ±2 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 0 V to 4.3 V; $V_{CC}$ = 0 V | | - | - | ±2 | µA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $V_{SW}$ = GND or $V_{CC}$; $V_{CC}$ = 4.3 V | | - | - | 2 | µA |
| $\Delta I_{CC}$ | additional supply current | $V_I$ = 1.8 V; $V_{SW}$ = GND or $V_{CC}$; $V_{CC}$ = 2.775 V | | - | - | 1.5 | µA |
| $C_I$ | input capacitance | pins S and OE | | - | 1.3 | - | pF |
| $C_{S(OFF)}$ | OFF-state capacitance | pins CLK1n, CLK2n, 1D1n 1D2n, 2D1n and 2D2n; $V_I$ = 0 V to 3.3 V | [2] | - | 3.0 | - | pF |
| $C_{S(ON)}$ | ON-state capacitance | pins CLKn, 1Dn and 2Dn; $V_I$ = 0 V to 3.3 V | [2] | - | 8.4 | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 2.775 V.

[2] n = + or –.

## 11.1 Test circuits




$V_I$ = $V_{CC}$ or GND and $V_O$ = GND or $V_{CC}$.

Test circuit also applies for 2Dn, 2D1n, 2D2n CLKn, CLK1n and CLK2n (n = + or –).

**Fig 4. Test circuit for measuring OFF-state leakage current**

## 11.2 ON resistance

**Table 8. ON resistance**

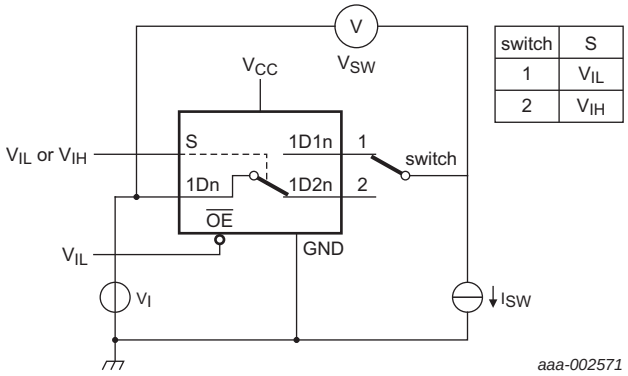
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| **low speed mode** | | | | | | | |
| $R_{ON}$ | ON resistance | $V_I$ = 1.2 V; $I_{SW}$ = 10 mA; see Figure 5 | | | | | |
| | | $V_{CC}$ = 2.65 V | | - | 7.5 | 14 | Ω |
| $\Delta R_{ON}$ | ON resistance mismatch between channels | $V_I$ = 1.2 V; $I_{SW}$ = 10 mA | [2] | | | | |
| | | $V_{CC}$ = 2.65 V | | - | 0.65 | - | Ω |
| **High speed mode** | | | | | | | |
| $R_{ON}$ | ON resistance | $V_I$ = 0.1 V; $I_{SW}$ = 10 mA; see Figure 5 | | | | | |
| | | $V_{CC}$ = 2.65 V | | - | 5.5 | 9.5 | Ω |
| $\Delta R_{ON}$ | ON resistance mismatch between channels | $V_I$ = 0.1 V; $I_{SW}$ = 10 mA | [2] | | | | |
| | | $V_{CC}$ = 2.65 V | | - | 0.65 | - | Ω |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

[2] Measured at identical $V_{CC}$, temperature and input voltage.

## 11.3 ON resistance test circuit and graphs




| switch | S |
|---|---|
| 1 | $V_{IL}$ |
| 2 | $V_{IH}$ |

$R_{ON} = V_{SW} / I_{SW}$.

Test circuit also applies for 2Dn, 2D1n, 2D2n CLKn, CLK1n and CLK2n (n = + or –).

**Fig 5. Test circuit for measuring ON resistance**

# 12. Dynamic characteristics

**Table 9. Dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 9.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = –40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $t_{pd}$ | propagation delay | CLKn to CLK1n or CLK2n; 1Dn to 1D1n or 1D2n or 2Dn to 2D1n or 2D2n; see Figure 6 | [2][3][4] | | | | |
| | | $V_{CC}$ = 2.775 V | | - | 0.25 | - | ns |
| $t_{en}$ | enable time | S or $\overline{OE}$ to CLKn, 1Dn or 2Dn; see Figure 7 | [2][3] | | | | |
| | | $V_{CC}$ = 2.65 V to 2.775 V | | - | 13.5 | 37 | ns |
| $t_{dis}$ | disable time | S or $\overline{OE}$ to CLKn, 1Dn or 2Dn; see Figure 7 | [2][3] | | | | |
| | | $V_{CC}$ = 2.65 V to 2.775 V | | - | 5.5 | 27 | ns |
| $t_{b-m}$ | break-before-make time | see Figure 8 | [4] | | | | |
| | | $V_{CC}$ = 2.65 V to 2.775 V | | 3 | 7 | - | ns |
| $t_{sk(p)}$ | pulse skew time | $V_{CC}$ = 2.65 V to 2.775 V; $V_{SW}$ = 0.2 V (p-p) | [4] | - | 10 | - | ps |
| $t_{sk(o)}$ | output skew time | $V_{CC}$ = 2.65 V to 2.775 V; $V_{SW}$ = 0.2 V (p-p) | [4] | - | 15 | - | ps |
| $t_{sk(pr)}$ | process skew time | $V_{CC}$ = 2.65 V to 2.775 V; $V_{SW}$ = 0.2 V (p-p) | [4] | - | 40 | - | ps |

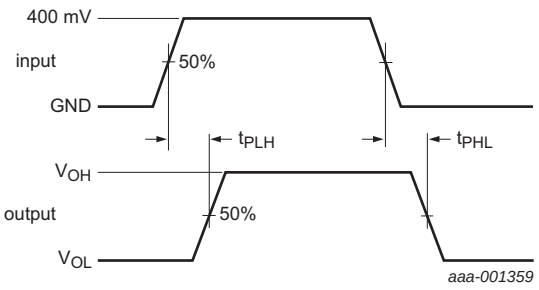
[1] Typical values are measured at $T_{amb}$ = 25 °C, $C_L$ = 5 pF and $V_{CC}$ = 2.775 V.

[2] n = + or –.

[3] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZH}$
$t_{dis}$ is the same as $t_{PHZ}$

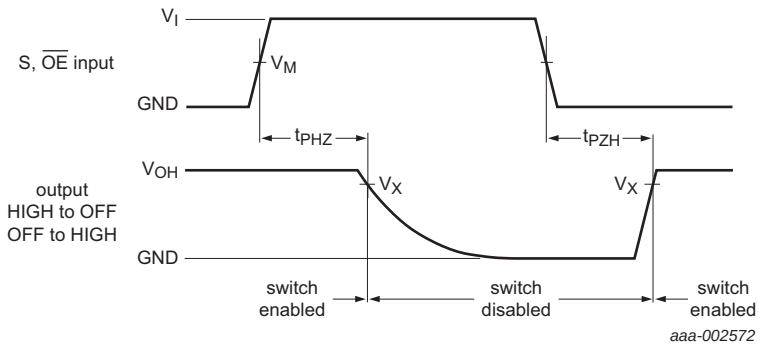
[4] Guaranteed by design.

## 12.1 Waveform and test circuits




Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.
$t_r = t_f \leq 500$ ps.

**Fig 6. The data input to output propagation delay times**



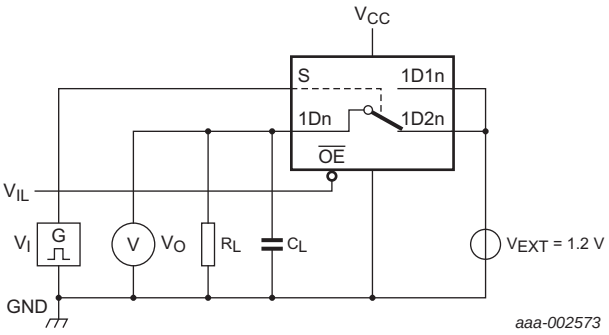

Measurement points are given in Table 10.

Logic level: $V_{OH}$ and $V_{OL}$ are typical output voltage levels that occur with the output load.

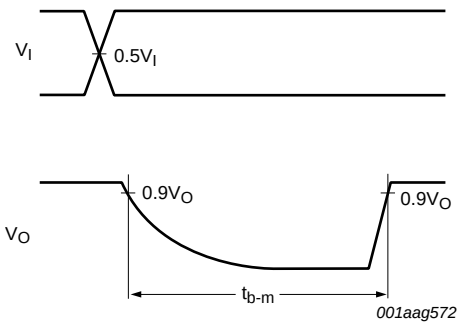
**Fig 7. Enable and disable times**

**Table 10. Measurement points**

| Supply voltage | Input | | Output |
|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_I$ | $V_X$ |
| 2.65 V to 2.775 V | $0.5V_{CC}$ | $V_{CC}$ | $0.9V_{OH}$ |



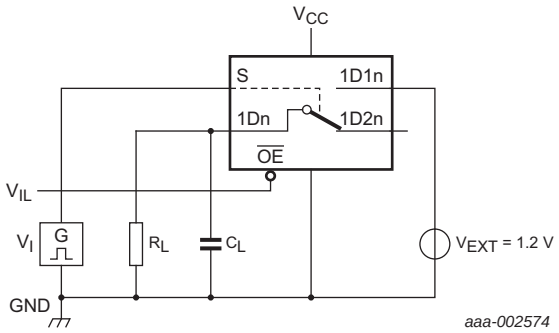

a. Test circuit.




b. Input and output measurement points

Test circuit also applies for 2Dn, 2D1n, 2D2n CLKn, CLK1n and CLK2n (n = + or −).

**Fig 8. Test circuit for measuring break-before-make timing**




Test circuit also applies for 2Dn, 2D1n, 2D2n CLKn, CLK1n and CLK2n (n = + or –).

Test data is given in Table 11.

Definitions test circuit:

$R_T$ = Termination resistance (should be equal to output impedance $Z_o$ of the pulse generator).

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$V_{EXT}$ = External voltage for measuring switching times.

$V_I$ may be connected to S or $\overline{OE}$.

**Fig 9. Test circuit for measuring switching times**

**Table 11. Test data**

| Supply voltage | Input | | Load | |
|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ |
| 2.65 V to 2.775 V | $V_{CC}$ | ≤ 2.5 ns | 5 pF | 50 Ω |

## 12.2 Additional dynamic characteristics

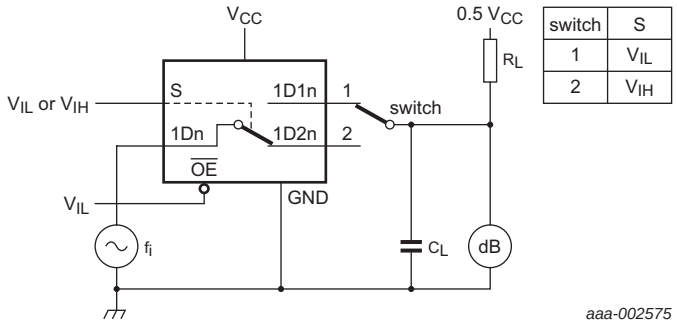
**Table 12. Additional dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I$ = GND or $V_{CC}$ (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = 25 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $f_{(-3dB)}$ | –3 dB frequency response | $R_L$ = 50 Ω; see Figure 10 | [1] | | | | |
| | | $C_L$ = 0 pF; $V_{CC}$ = 2.775 V | | - | 950 | - | MHz |
| $\alpha_{iso}$ | isolation (OFF-state) | $f_i$ = 100 MHz; $R_L$ = 50 Ω; see Figure 11 | [1] | | | | |
| | | $V_{CC}$ = 2.775 V | | - | –35 | - | dB |
| Xtalk | crosstalk | between switches; $f_i$ = 100 MHz; $R_L$ = 50 Ω; see Figure 12 | [1] | | | | |
| | | $V_{CC}$ = 2.775 V | | - | –55 | - | dB |

[1] $f_i$ is biased at $0.5V_{CC}$.

## 12.3 Test circuits

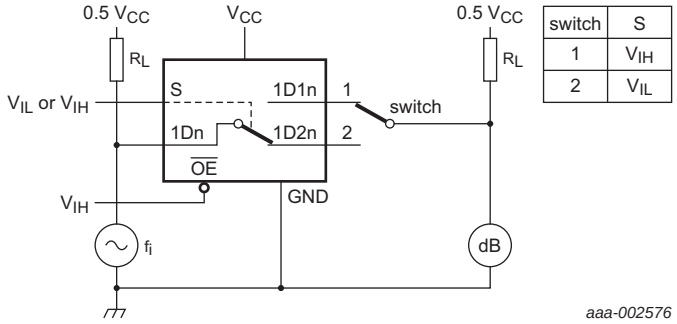



| switch | S |
|---|---|
| 1 | $V_{IL}$ |
| 2 | $V_{IH}$ |

Adjust $f_i$ voltage to obtain 0 dBm level at output. Increase $f_i$ frequency until dB meter reads −3 dB.

Test circuit also applies for 2Dn, 2D1n, 2D2n CLKn, CLK1n and CLK2n (n = + or −).

**Fig 10. Test circuit for measuring the frequency response when channel is in ON-state**

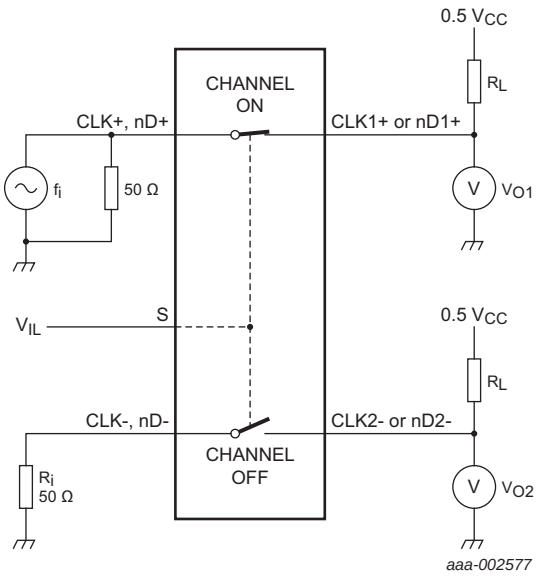



| switch | S |
|---|---|
| 1 | $V_{IH}$ |
| 2 | $V_{IL}$ |

Adjust $f_i$ voltage to obtain 0 dBm level at input.

Test circuit also applies for 2Dn, 2D1n, 2D2n CLKn, CLK1n and CLK2n (n = + or −).

**Fig 11. Test circuit for measuring isolation (OFF-state)**

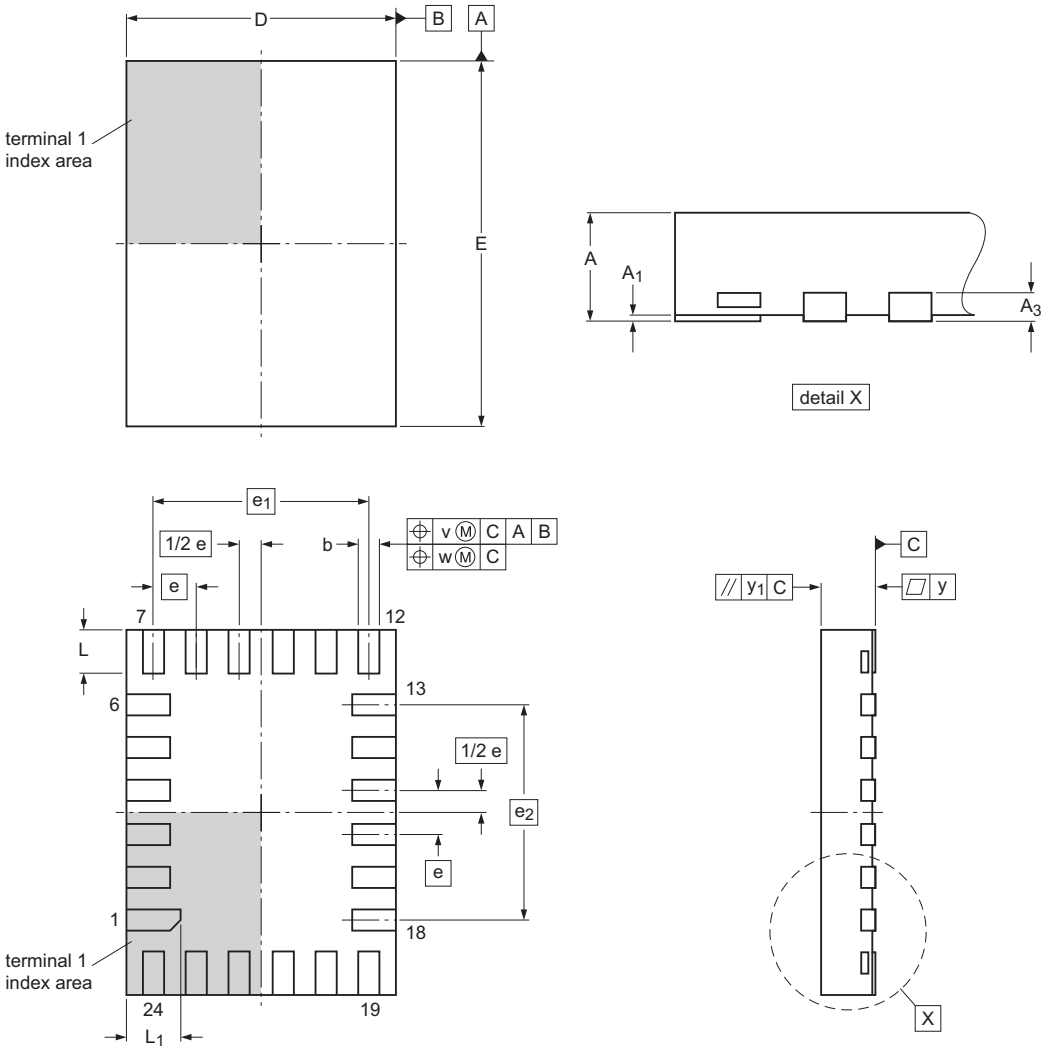



$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

**Fig 12. Test circuit for measuring crosstalk between switches**

## 13. Package outline

**XQFN24: plastic, extremely thin quad flat package; no leads; 24 terminals; body 2.5 x 3.4 x 0.5 mm** **SOT1310-1**




Dimensions

| Unit | | A | $A_1$ | b | $A_3$ | D | E | e | $e_1$ | $e_2$ | L | $L_1$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.5 | 0.05 | 0.25 | | 2.6 | 3.5 | | | | 0.45 | 0.55 | | | | |
| | nom | | | 0.20 | 0.127 | 2.5 | 3.4 | 0.4 | 2.0 | 2.0 | 0.40 | 0.50 | 0.10 | 0.05 | 0.05 | 0.05 |
| | min | | 0.00 | 0.15 | | 2.4 | 3.3 | | | | 0.35 | 0.45 | | | | |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

*sot1310-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1310-1 | | MO-288 | | | | ~~11-07-19~~ 11-08-18 |

**Fig 13. Package outline SOT1310-1 (XQFN24)**

## 14. Abbreviations

**Table 13. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| NX3DV642 v.1 | 20120820 | Product data sheet | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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