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# FDC3512

# 80V N-Channel PowerTrench® MOSFET

### **General Description**

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low R<sub>DS(ON)</sub> and fast switching speed.

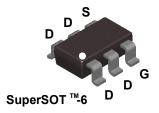
#### **Applications**

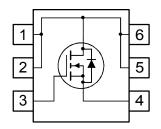
• DC/DC converter

#### **Features**

• 3.0 A, 80 V  $R_{DS(ON)} = 77 \text{ m}\Omega$  @  $V_{GS} = 10 \text{ V}$  $R_{DS(ON)} = 88 \text{ m}\Omega$  @  $V_{GS} = 6 \text{ V}$ 

- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS}(\mbox{\scriptsize ON})}$
- Low gate charge (13nC typ)
- High power and current handling capability
- Fast switching speed





### Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
$V_{DSS}$	Drain-Source Voltage		80	V
V <sub>GSS</sub>	Gate-Source Voltage		± 20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	3.0	А
	- Pulsed		20	
$P_D$	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
Reic	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
 .352	FDC3512	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-So	urce Avalanche Ratings (Note	2)				•
W <sub>DSS</sub>	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 40 \text{ V}$ , $I_D = 3.0 \text{ A}$			90	mJ
I <sub>AR</sub>	Drain-Source Avalanche Current				3.0	Α
Off Char	acteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	80			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C		80		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2	2.4	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-6		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On Resistance	$V_{GS} = 10 \text{ V}, \ I_D = 3.0 \text{ A}$ $V_{GS} = 6.0 \text{ V}, \ I_D = 2.8 \text{ A}$ $V_{GS} = 10 \text{ V}, \ I_D = 3.0 \text{ A}; T_J = 125^{\circ}\text{C}$		56 61 97	77 88 141	mΩ
I <sub>D(on)</sub>	On–State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	10			Α
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V},  I_{D} = 3.0 \text{ A}$		14		S
Dynamic	Characteristics		•		•	•
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 40 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		634		pF
Coss	Output Capacitance	f = 1.0 MHz		58		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	_		28		pF
Switchin	g Characteristics (Note 2)				•	
t <sub>d(on)</sub>	Turn–On Delay Time	$V_{DD} = 40 \text{ V}, \qquad I_{D} = 1 \text{ A},$		7	14	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		3	6	ns
$t_{d(off)}$	Turn-Off Delay Time			24	28	ns
t <sub>f</sub>	Turn-Off Fall Time	1		4	8	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 40 \text{ V}, \qquad I_{D} = 3.0 \text{ A},$		13	18	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		2.4		nC
$Q_{gd}$	Gate-Drain Charge	]		2.8		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				1.3	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2)		0.8	1.2	V
m .	Diode Reverse Recovery Time	$I_F = 3.0 \text{ A},$		28.2		nS
Q <sub>rr</sub>	Diode Reverse Recovery Charge	$d_{iF}/d_t = 300 \text{ A/}\mu\text{s}$ (Note 2)		48		nC

### Notes:

- 1.  $R_{\theta,JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta,JC}$  is guaranteed by design while  $R_{\theta,CA}$  is determined by the user's board design.
  - a. 78°C/W when mounted on a 1in² pad of 2oz copper on FR-4 board.
  - b. 156°C/W when mounted on a minimum pad.
- 2. Pulse Test: Pulse Width  $\leq 300~\mu s,~Duty~Cycle \leq 2.0\%$

# **Typical Characteristics**

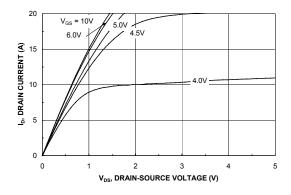
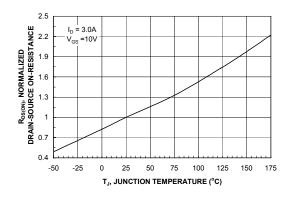


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



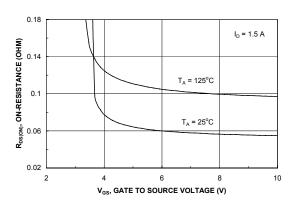
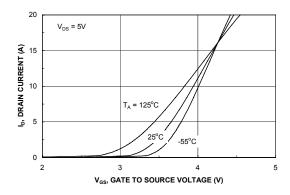


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



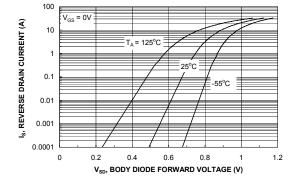
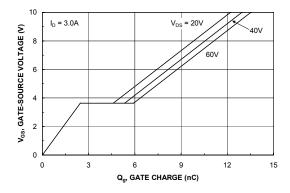


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



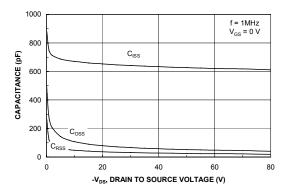
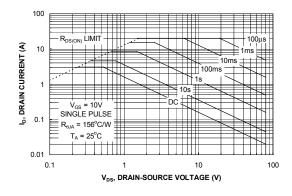


Figure 7. Gate Charge Characteristics.





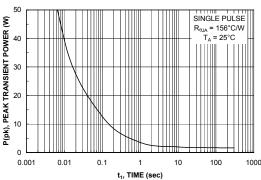


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

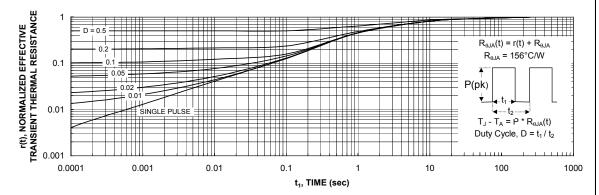


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

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