# 35V/3.2A Multicell Lithium-Ion Step-Down Battery Charger with PowerPath and I²C Telemetry

## FEATURES

- **Li-Ion/Polymer Battery Charger with Termination**
- **Wide Charging Input Voltage Range: 4.5V to 35V**
- **High Efficiency Synchronous Operation**
- **16-Bit Digital Telemetry System Monitors $V_{BAT}$, $I_{BAT}$, $R_{BAT}$, $T_{BAT}$, $T_{DIE}$, $V_{IN}$, $I_{IN}$, $V_{OUT}$**
- **Charges 1-8 Lithium-Ion/Polymer Cells**
- Input Undervoltage Charge Current Limit Loop
- Input MPPT for Solar Panel Inputs
- Input Current Limit Prioritizes System Load Output
- Low Loss PowerPath™
- Instant-On Operation with Discharged or Missing Battery
- JEITA Temperature Controlled Charging
- Pin Compatible with LiFePO$_4$ and SLA Versions

## APPLICATIONS

- Medical Instruments
- USB-C Power Delivery
- Industrial Handhelds
- Ruggedized Notebooks
- Tablet Computers

## DESCRIPTION

The LTC®4162-L is an advanced monolithic synchronous step-down switching battery charger and PowerPath™ manager that seamlessly manages power distribution between input sources such as wall adapters, backplanes, solar panels, etc., and a rechargeable Lithium-Ion/Polymer battery.

A high resolution measurement system provides extensive telemetry information for circuit voltages, currents, battery resistance and temperature which can all be read back over the I²C port. The I²C port can also be used to configure many charging parameters including charging voltages and currents, termination algorithms and numerous system status alerts.

The LTC4162-L can charge Lithium-Ion cell stacks from 1 cell to 8 cells with as much as 3.2A of charge current.

The power path topology decouples the output voltage from the battery allowing a portable product to start up instantly under very low battery voltage conditions.

The LTC4162-L is available in a thermally enhanced 28-pin 4mm × 5mm × 0.75mm QFN surface mount package.

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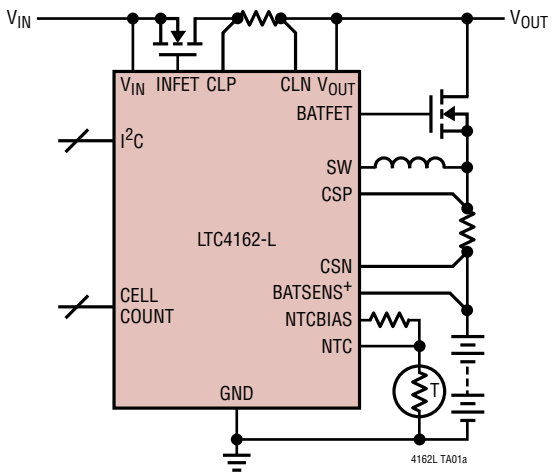
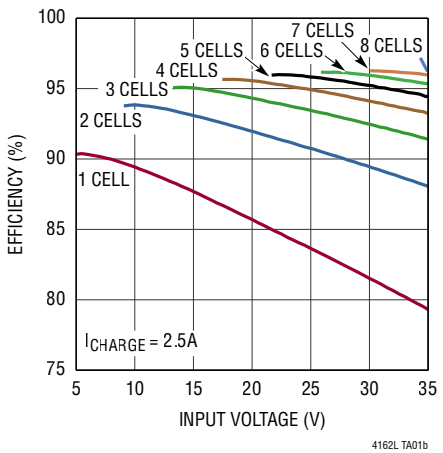
## TYPICAL APPLICATION

**1-8 Cell, 3.2A Step-Down Switching Battery Charger with PowerPath**




**Charging Efficiency vs Input Voltage by Cell Count**



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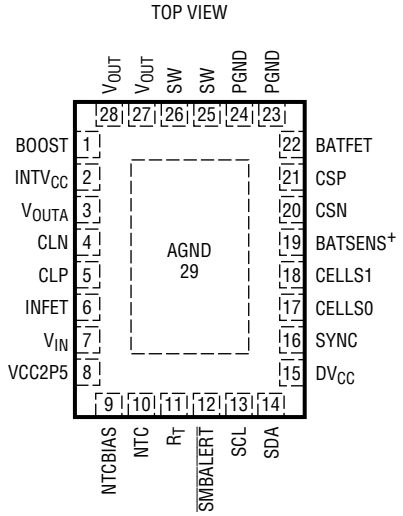
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

BATSENS+, $V_{IN}$, CSP, CSN, CLP, CLN, $V_{OUT}$, $V_{OUTA}$..... –0.3V to 36V
CSP to CSN, CLP to CLN.....±0.3V
CELLSO, CELLS1, SYNC ..... –0.3V to INTVCC
$DV_{CC}$ ..... –0.3V to 5.5V
SDA, SCL, $\overline{SMBALERT}$..... –0.3V to $DV_{CC}$
$I_{SW}$ ..... ±3.5A
Operating Junction Temperature Range (Notes 2, 4).....–40 to 125°C
Storage Temperature Range .....–65 to 150°C

## PIN CONFIGURATION




UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W, $\theta_{JC}$ = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| PART NUMBER | PART MARKING* | TAPE AND REEL | TEMP GRADE | DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|---|
| LTC4162EUFD-LAD#PBF | 4162A | | E | $I^2C$ Adjustable Voltage | –40°C to 125°C |
| LTC4162EUFD-L40#PBF | 4162B | | E | 4.0V Fixed Voltage | –40°C to 125°C |
| LTC4162EUFD-L41#PBF | 4162C | | E | 4.1V Fixed Voltage | –40°C to 125°C |
| LTC4162EUFD-L42#PBF | 4162D | | E | 4.2V Fixed Voltage | –40°C to 125°C |
| LTC4162EUFD-LADM#PBF | 4162K | | E | $I^2C$ Adjustable Voltage MPPT ON | –40°C to 125°C |
| LTC4162EUFD-L40M#PBF | 4162L | | E | 4.0V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162EUFD-L41M#PBF | 4162M | | E | 4.1V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162EUFD-L42M#PBF | 4162N | | E | 4.2V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162EUFD-LAD#TRPBF | 4162A | ✓ | E | $I^2C$ Adjustable Voltage | –40°C to 125°C |
| LTC4162EUFD-L40#TRPBF | 4162B | ✓ | E | 4.0V Fixed Voltage | –40°C to 125°C |
| LTC4162EUFD-L41#TRPBF | 4162C | ✓ | E | 4.1V Fixed Voltage | –40°C to 125°C |
| LTC4162EUFD-L42#TRPBF | 4162D | ✓ | E | 4.2V Fixed Voltage | –40°C to 125°C |
| LTC4162EUFD-LADM#TRPBF | 4162K | ✓ | E | $I^2C$ Adjustable Voltage MPPT ON | –40°C to 125°C |
| LTC4162EUFD-L40M#TRPBF | 4162L | ✓ | E | 4.0V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162EUFD-L41M#TRPBF | 4162M | ✓ | E | 4.1V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162EUFD-L42M#TRPBF | 4162N | ✓ | E | 4.2V Fixed Voltage MPPT ON | –40°C to 125°C |

# ORDER INFORMATION

| PART NUMBER | PART MARKING* | TAPE AND REEL | TEMP GRADE | DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|---|
| LTC4162IUFD-LAD#PBF | 4162A | | I | $I^2C$ Adjustable Voltage | –40°C to 125°C |
| LTC4162IUFD-L40#PBF | 4162B | | I | 4.0V Fixed Voltage | –40°C to 125°C |
| LTC4162IUFD-L41#PBF | 4162C | | I | 4.1V Fixed Voltage | –40°C to 125°C |
| LTC4162IUFD-L42#PBF | 4162D | | I | 4.2V Fixed Voltage | –40°C to 125°C |
| LTC4162IUFD-LADM#PBF | 4162K | | I | $I^2C$ Adjustable Voltage MPPT ON | –40°C to 125°C |
| LTC4162IUFD-L40M#PBF | 4162L | | I | 4.0V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162IUFD-L41M#PBF | 4162M | | I | 4.1V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162IUFD-L42M#PBF | 4162N | | I | 4.2V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162IUFD-LAD#TRPBF | 4162A | ✓ | I | $I^2C$ Adjustable Voltage | –40°C to 125°C |
| LTC4162IUFD-L40#TRPBF | 4162B | ✓ | I | 4.0V Fixed Voltage | –40°C to 125°C |
| LTC4162IUFD-L41#TRPBF | 4162C | ✓ | I | 4.1V Fixed Voltage | –40°C to 125°C |
| LTC4162IUFD-L42#TRPBF | 4162D | ✓ | I | 4.2V Fixed Voltage | –40°C to 125°C |
| LTC4162IUFD-LADM#TRPBF | 4162K | ✓ | I | $I^2C$ Adjustable Voltage MPPT ON | –40°C to 125°C |
| LTC4162IUFD-L40M#TRPBF | 4162L | ✓ | I | 4.0V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162IUFD-L41M#TRPBF | 4162M | ✓ | I | 4.1V Fixed Voltage MPPT ON | –40°C to 125°C |
| LTC4162IUFD-L42M#TRPBF | 4162N | ✓ | I | 4.2V Fixed Voltage MPPT ON | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

# ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 4). $V_{IN}$ = 18V, $DV_{CC}$ = 3.3V, $R_{SNSI}$ = 10mΩ, $R_{SNSB}$ = 10mΩ unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **System Voltages and Currents** | | | | | | | |
| $V_{IN}$ | Input Supply Voltage | | ● | 4.5 | | 35 | V |
| $V_{BAT}$ | Battery Voltage | | ● | 2.7 | | 35 | V |
| $I_{BATSENS+}$ | Battery Drain Current | $V_{IN} – V_{BATSENS+} > V_{IN_DUVLO}$, Terminated<br>$V_{IN} – V_{BATSENS+} < V_{IN_DUVLO}$<br>$V_{IN}$ = 0, SHIPMODE Activated | | | 0.5<br>54<br>2.8 | 1<br>100<br>5 | µA<br>µA<br>µA |
| $I_{VIN}$ | $V_{IN}$ Drain Current | $V_{IN} – V_{BATSENS+} > V_{IN_DUVLO}$, Terminated | | | 115 | 200 | µA |
| **Switching Battery Charger** | | | | | | | |
| $V_{CHARGE}$ | Range<br>Resolution (5 Bits)<br>Accuracy | Per cell_count | <br><br>● | | 3.8125–4.2<br>12.5<br>–0.5<br>–1.5 | <br><br>0.5<br>1.5 | V<br>mV<br>%<br>% |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 4). $V_{IN}$ = 18V, DVCC = 3.3V, $R_{SNSI}$ = 10mΩ, RSNSB = 10mΩ unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{CHARGE}$<br>Servo Voltage<br>($V_{CSP}$ – $V_{CSN}$) | Range<br>Resolution (5 Bits)<br>Accuracy | $I_{CHARGE}$ = ($V_{CSP}$ – $V_{CSN}$)/$R_{SNSB}$<br>Note 5 | <br><br><br>● | <br><br>–0.25<br>–0.75 | 1–32<br>1<br><br> | <br><br>0.25<br>0.75 | mV<br>mV<br>mV<br>mV |
| $I_{INLIM}$<br>Servo Voltage<br>($V_{CLP}$ – $V_{CLN}$) | Range<br>Resolution (6 Bits)<br>Accuracy | $I_{IN}$ = ($V_{CLP}$ – $V_{CLN}$)/$R_{SNSI}$<br>Note 6 | <br><br> | <br><br>–0.2 | 0.5–32<br>0.5<br> | <br><br>0.2 | mV<br>mV<br>mV |
| $V_{INLIM}$ | Range<br>Resolution (8 Bits)<br>Full Scale Accuracy | | <br><br> | <br><br>–1 | 0.14–36<br>140.625<br> | <br><br>1 | V<br>mV<br>% |
| $f_{OSC}$ | Switching Frequency | $R_T$ = 63.4k | ● | 1.4 | 1.5 | 1.6 | MHz |
| $D_{MAX}$ | Maximum Duty Cycle | | | | 99.5 | | % |
| $R_{SWITCH}$ | Primary Switch On-Resistance | | | | 90 | | mΩ |
| $R_{RECT}$ | Rectifier Switch On-Resistance | | | | 90 | | mΩ |
| $I_{PEAK}$ | Peak Inductor Current Limit | Note 3 | | | 45mV/$R_{SNSB}$ | | A |
| **System Controls** | | | | | | | |
| $V_{IN_UVLO}$ | $V_{IN}$ Charger Enable<br>Input Undervoltage Lockout | Rising Threshold<br>Hysteresis | | 4.2 | 4.4<br>0.2 | 4.6 | V<br>V |
| $V_{IN_DUVLO}$ | $V_{IN}$ to BATSENS+ Charger Enable<br>Differential Undervoltage Lockout | Rising Threshold<br>Hysteresis | | 100 | 150<br>170 | 200 | mV<br>mV |
| $V_{IN_OVLO}$ | $V_{IN}$ Charger Disable<br>Overvoltage Lockout | Rising Threshold<br>Hysteresis | | 37.6 | 38.6<br>1.4 | 40 | V<br>V |
| $V_{INTVCC_UVLO}$ | $INTV_{CC}$ Telemetry Enable<br>Undervoltage Lockout | Rising Threshold<br>Hysteresis | | 2.75 | 2.85<br>0.12 | 2.95 | V<br>V |
| **Telemetry A/D Measurement Subsystem** | | | | | | | |
| $I_{BAT}$<br>($V_{CSP}$ – $V_{CSN}$) | Resolution<br>Offset Error<br>Span Error | $I_{BAT}$ = ($V_{CSP}$ – $V_{CSN}$)/$R_{SNSB}$<br>0.32mV < $V_{CSP}$ – $V_{CSN}$ < 32mV | | <br>–0.15<br>–1.25 | 1.466<br><br> | <br>0.15<br>1.25 | µV /LSB<br>mV<br>%rdng |
| $I_{IN}$<br>($V_{CLP}$ – $V_{CLN}$) | Resolution<br>Offset Error<br>Span Error | $I_{IN}$ = ($V_{CLP}$ – $V_{CLN}$)/$R_{SNSI}$<br>0.32mV < $V_{CLP}$ – $V_{CLN}$ < 32mV | | <br>–0.15<br>–1.25 | 1.466<br><br> | <br>0.15<br>1.25 | µV/LSB<br>mV<br>%rdng |
| $V_{IN}$ | Resolution<br>Offset Error<br>Span Error | 3V < $V_{IN}$ < 35V | | <br>–25<br>–1 | 1.649<br><br> | <br>25<br>1 | mV/LSB<br>mV<br>%rdng |
| $V_{BATSENS+}$<br>(Per cell_count) | Resolution<br>Offset Error<br>Span Error | 2V < $V_{BATSENS+}$ < 4.2V | | <br>–10<br>–1 | 192.4<br><br> | <br>10<br>1 | µV/LSB<br>mV<br>%rdng |
| $V_{OUT}$ | Resolution<br>Offset Error<br>Span Error | 3V < $V_{OUT}$ < 35V | | <br>–25<br>–1 | 1.653<br><br> | <br>25<br>1 | mV/LSB<br>mV<br>%rdng |
| $V_{NTC}/V_{NTCBIAS}$ | Resolution<br>Offset Error<br>Span Error | 0 < $V_{NTC}/V_{NTCBIAS}$ < 1 | | <br>–1<br>–1 | 45.833<br><br> | <br>1<br>1 | µV/V/LSB<br>mV/V<br>%rdng |
| T_die | Resolution<br>Offset | | | | 0.0215<br>–264.4 | | °C/LSB<br>°C |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 4). $V_{IN}$ = 18V, DVCC = 3.3V, $R_{SNSI}$ = 10mΩ, RSNSB = 10mΩ unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Serial Port, SDA, SCL, $\overline{\text{SMBALERT}}$** | | | | | | | |
| $DV_{CC}$ | Logic Reference Level | | ● | 1.8 | | 5.5 | V |
| $I_{DVCCQ}$ | $DV_{CC}$ Current | SCL/SDA = $DV_{CC}$, 0kHz | | | 0 | | µA |
| ADDRESS | $I^2C$ Address | | | | 0b1101000[R/W] | | |
| $V_{IHI2C}$ | Input High Threshold | | | 70 | | | % $DV_{CC}$ |
| $V_{ILI2C}$ | Input Low Threshold | | | | | 30 | % $DV_{CC}$ |
| $V_{OLI2C}$ | Digital Output Low (SDA/$\overline{\text{SMBALERT}}$) | $I_{SDA/\overline{SMBALERT}}$ = 3mA | | | | 400 | mV |
| $F_{SCL}$ | SCL Clock Frequency | | | | | 400 | kHz |
| $t_{LOW}$ | LOW Period of SCL Clock | | | 1.3 | | | µs |
| $t_{HIGH}$ | HIGH Period of SCL Clock | | | 0.6 | | | µs |
| $t_{BUF}$ | Bus Free Time Between Start and Stop Conditions | | | 1.3 | | | µs |
| $t_{HD,STA}$ | Hold Time, After (Repeated) Start Condition | | | 0.6 | | | µs |
| $t_{SU,STA}$ | Setup Time after a Repeated Start Condition | | | 0.6 | | | µs |
| $t_{SU,STO}$ | Stop Condition Set-Up Time | | | 0.6 | | | µs |
| $t_{HD,DAT(OUT)}$ | Output Data Hold Time | | | 0 | | 900 | ns |
| $t_{HD,DAT(IN)}$ | Input Data Hold Time | | | 0 | | | ns |
| $t_{SU,DAT}$ | Data Set-Up Time | | | 100 | | | ns |
| $t_{SP}$ | Input Spike Suppression Pulse Width | | | | | 50 | ns |
| **SYNC Pin** | | | | | | | |
| VIHSYNC | Input High Threshold | | ● | 1.5 | | | V |
| VILSYNC | Input Low Threshold | | ● | | | 0.2 | V |
| **Pin Leakages (NTC, CELLS0, CELLS1, SDA, SCL, SYNC, $\overline{\text{SMBALERT}}$)** | | | | | | | |
| | Pin Current | | | –50 | | 50 | nA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC4162 includes over-temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

**Note 3:** The safety current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current may result in device degradation or failure.

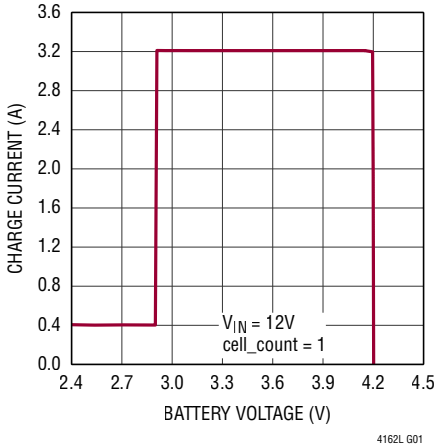
**Note 4:** The E-grade is tested under pulsed load conditions such that $T_J \approx T_A$. The E-grade is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The I-grade is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature ($T_J$) is calculated from the ambient temperature ($T_A$) and power dissipation ($P_D$) according to the formula $T_J = T_A + (P_D \bullet \theta J_A)$. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

**Note 5:** Charge Current is given by the charger servo voltage, $V_{CSP-CSN}$, divided by the charge current setting resistor $R_{SNSB}$. Errors in the value of the external resistor contribute directly to the total charge current error.

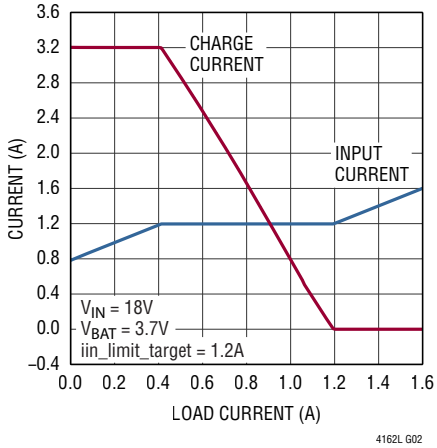
**Note 6:** Input Current is given by the $V_{CLP-CLN}$ servo voltage divided by the input current setting resistor $R_{SNSI}$. Errors in the value of the external resistor contribute directly to the total input current error.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

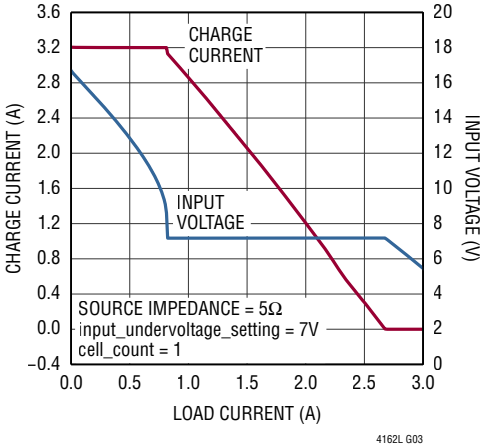
### Charge Current vs Battery Voltage



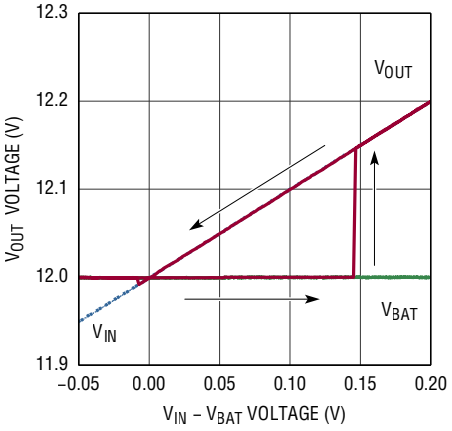

### Input Current and Charge Current vs Load Current



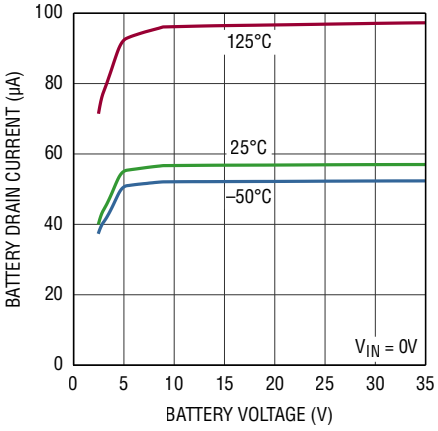

### Resistive Source Input Voltage and Charge Current vs Load Current



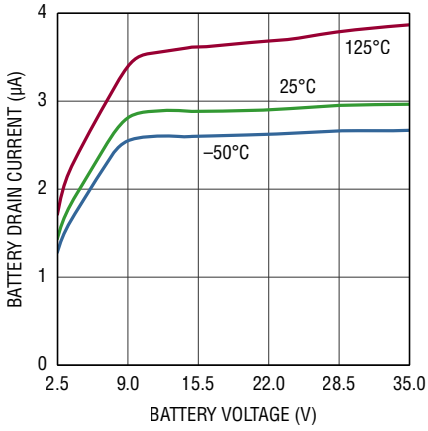

### VOUT vs VIN Power Path Controller



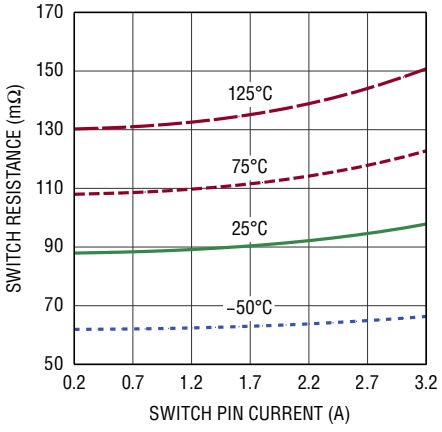

### No Input Battery Drain Current vs Battery Voltage



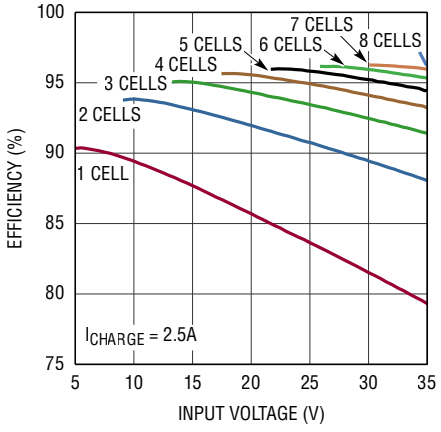

### Ship Mode Battery Drain Current vs Battery Voltage



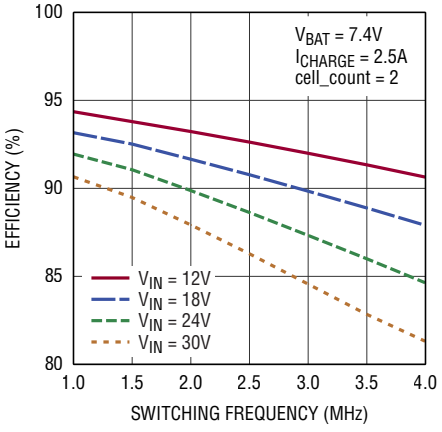

### Top and Bottom Switch $R_{DS(ON)}$




### Efficiency vs Input Voltage

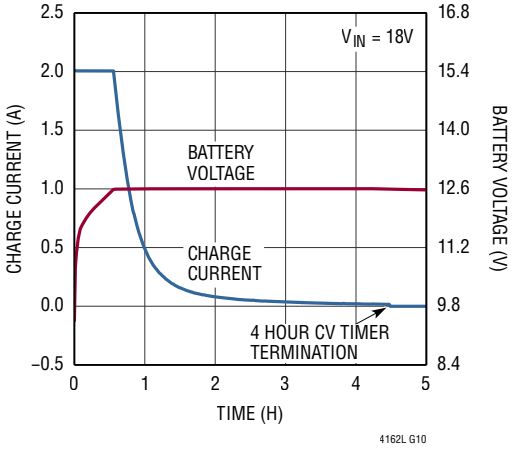



### Efficiency vs Switching Frequency

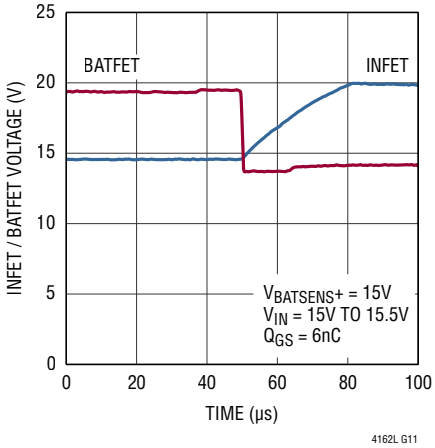


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

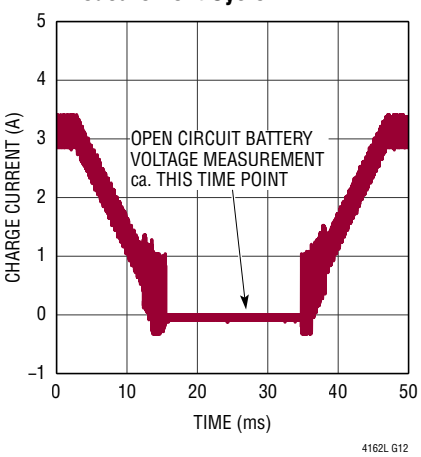
### 2.2Ah 3-Cell Battery Charge Current and Voltage vs Time



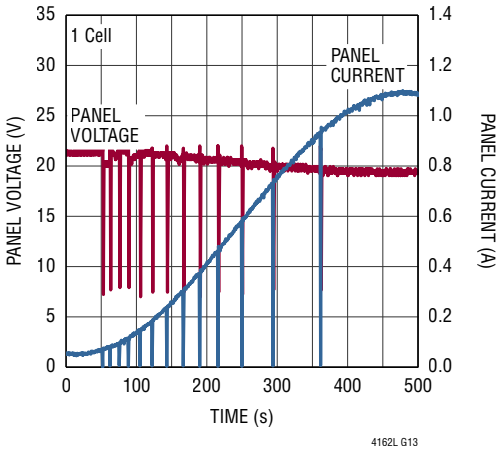

### Example Power Path Handover



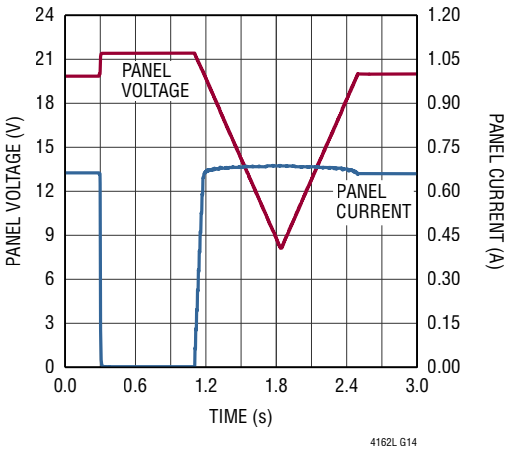

### Charge Current During BSR Measurement Cycle



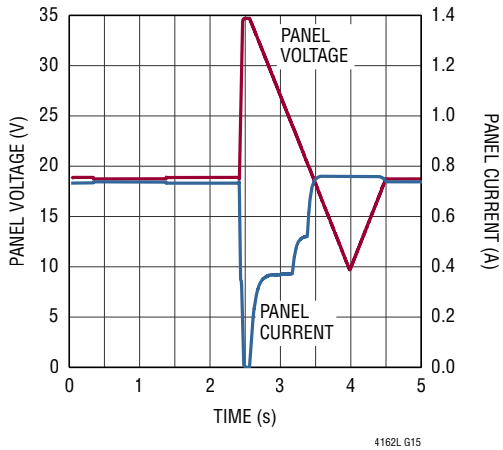

### Light to Dark Solar Panel Tracking



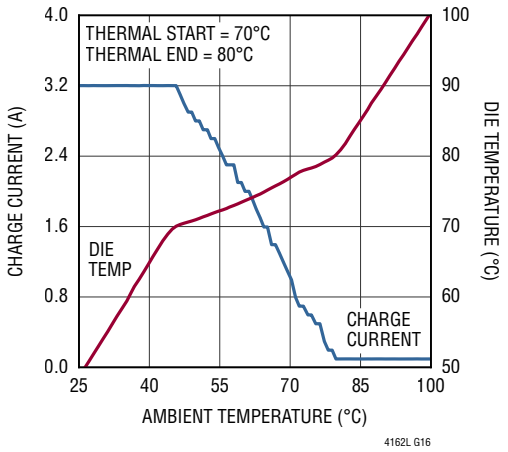

### Solar Panel Global Sweep




### Multi-Peak Solar Panel Acquisition

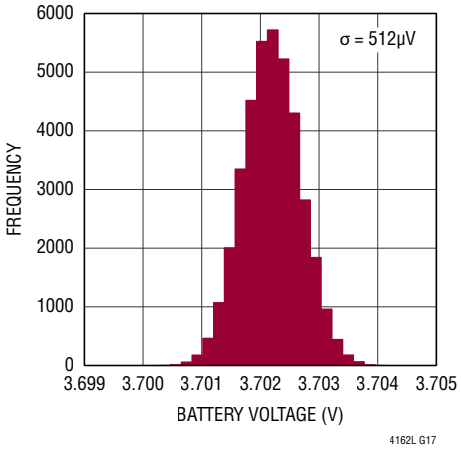



### Charge Current and Die Temperature Using Thermal Regulation

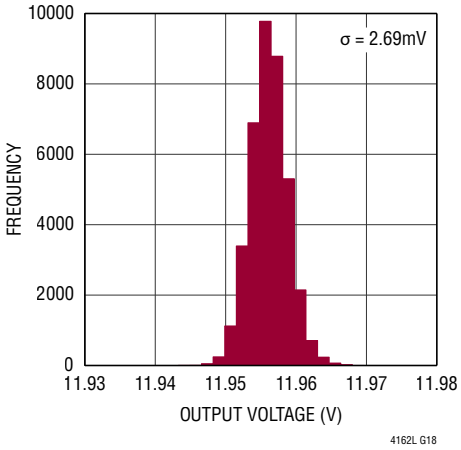


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

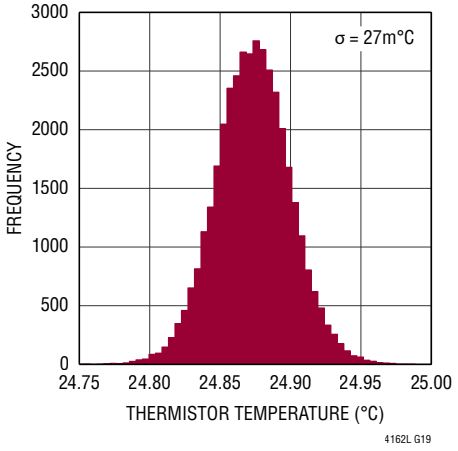
**Histogram of vbat Readings**



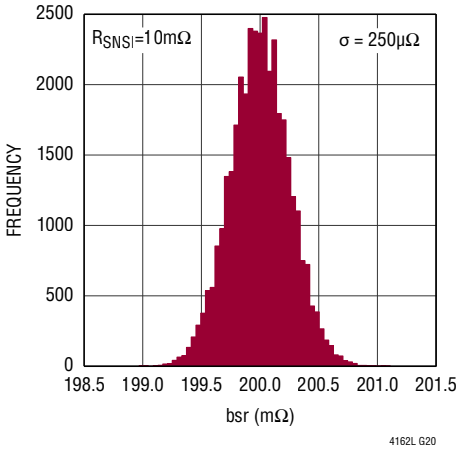

**Histogram of vout Readings**



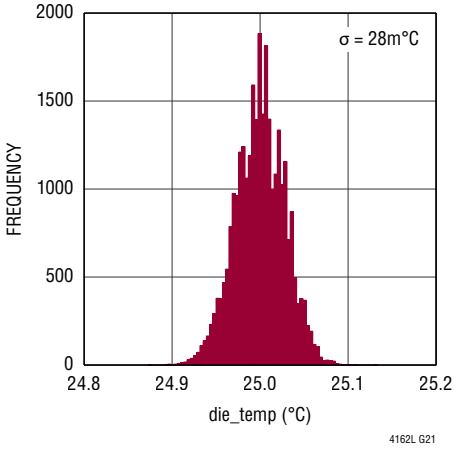

**Histogram of thermistor_voltage Readings**



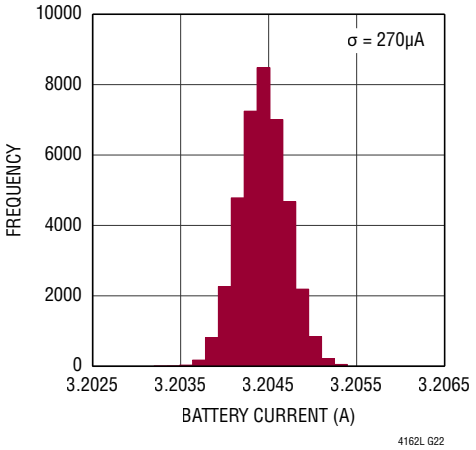

**Histogram of bsr Readings**



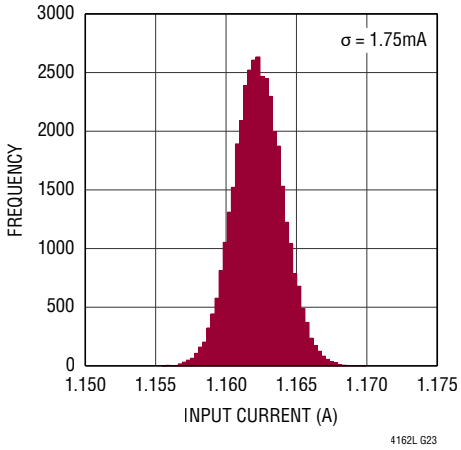

**Histogram of die_temp Readings**



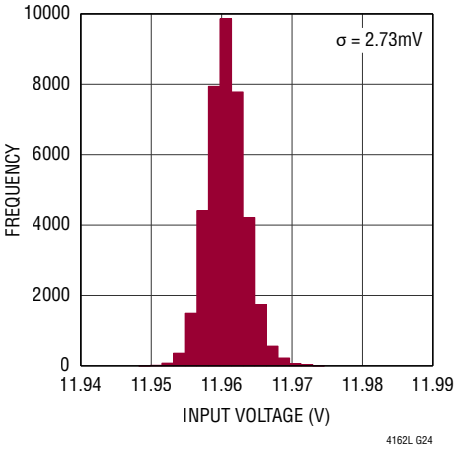

**Histogram of ibat Readings**




**Histogram of iin Readings**




**Histogram of vin Readings**



## PIN FUNCTIONS

**BOOST (Pin 1):** Gate-Drive bias for the high side switch in the switching regulator. This pin provides a pumped bias voltage relative to SW. The voltage on this pin is charged up through an internal diode from $INTV_{CC}$. A 22nF multilayer ceramic capacitor is required from SW to BOOST.

**$INTV_{CC}$ (Pin 2):** Bypass pin for the internal 5V regulator. This regulator provides power to the internal analog circuitry. A 4.7µF multilayer ceramic capacitor is required from $INTV_{CC}$ to GND.

**$V_{OUTA}$ (Pin 3):** Analog system power pin. $V_{OUTA}$ powers the majority of circuits on the LTC4162. A 0.1µF multilayer ceramic capacitor is required from $V_{OUTA}$ to GND.

**CLN (Pin 4):** Connection point for the negative terminal of the sense resistor that measures and regulates input current by limiting charge current.

**CLP (Pin 5):** Connection point for the positive terminal of the sense resistor that measures and regulates input current by limiting charge current.

**INFET (Pin 6):** Gate control output pin for an input reverse blocking external N-channel MOSFET between $V_{IN}$ and $V_{OUT}$.

**$V_{IN}$ (Pin 7):** Supply voltage detection and INFET charge pump supply for the INFET/BATFET PowerPath. When voltage at $V_{IN}$ is detected as being high enough to charge a battery, the INFET charge-pump is activated and the BATFET charge-pump is deactivated thereby powering $V_{OUTA}$ from the input supply through an external NMOS transistor and also starting a charge cycle. A 0.1µF multilayer ceramic capacitor is required from $V_{IN}$ to GND.

**VCC2P5 (Pin 8):** Bypass pin for the internal 2.5V regulator. This regulator provides power to the internal logic circuitry. A 1µF multilayer ceramic capacitor is required from VCC2P5 to GND.

**NTCBIAS (Pin 9):** NTC thermistor bias output. Connect a low temperature coefficient bias resistor between NTCBIAS and NTC, and a thermistor between NTC and GND. The bias resistor should be equal in value to the nominal value of the thermistor. The LTC4162 applies 1.2V to this pin during NTC measurement and expects a thermistor β value of 3490K. Higher β value thermistors can be used with simple circuit modifications.

**NTC (Pin 10):** Thermistor input. The NTC pin connects to a negative temperature coefficient thermistor to monitor the temperature of the battery. The voltage on this pin is digitized by the analog to digital converter to qualify battery charging and is available for readout via the $I^2C$ port. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground.

**$R_T$ (Pin 11):** Switching regulator frequency control pin. The $R_T$ pin controls the switching regulator's internal oscillator frequency by placing a resistor from $R_T$ to GND.

**$\overline{\text{SMBALERT}}$ (Pin 12):** Interrupt output. This open drain output pulls low when one or more of the programmable alerts is triggered.

**SCL (Pin 13):** Open drain clock input for the $I^2C$ port. The $I^2C$ port input levels are scaled with respect to $DV_{CC}$ for $I^2C$ compliance.

**SDA (Pin 14):** Open drain data input/output for the $I^2C$ port. The $I^2C$ port input levels are scaled with respect to $DV_{CC}$ for $I^2C$ compliance.

**$DV_{CC}$ (Pin 15):** Logic supply for the $I^2C$ port. $DV_{CC}$ sets the reference level of the SDA and SCL pins for $I^2C$ compliance. It should be connected to the same power supply as the SDA and SCL pull up resistors.

**SYNC (Pin 16):** Optional external clock input for the switching battery charger. The switching battery charger will lock to a square wave or pulse on this pin that is close to the frequency programmed by the $R_T$ pin. Ground SYNC if this feature is not needed.

## PIN FUNCTIONS

**CELLS0 (Pin 17):** Cell count selection pin. Used in combination with CELLS1, this pin sets the total number of series cells to be charged. The pin should be strapped to either $INTV_{CC}$, VCC2P5 or GND to represent one of three possible states. See Table 5.

**CELLS1 (Pin 18):** Cell count selection pin. Used in combination with CELLS0, this pin sets the total number of series cells to be charged. The pin should be strapped to either $INTV_{CC}$, VCC2P5 or GND to represent one of three possible states. See Table 5.

**BATSENS+ (Pin 19):** Positive terminal battery sense pin. BATSENS+ should Kelvin sense the positive terminal of the battery for optimized charging. A 10µF multilayer ceramic capacitor is required from BATSENS+ to ground.

**CSN (Pin 20):** Connection point for the negative terminal of the current sense resistor used to measure and limit charge current.

**CSP (Pin 21):** Connection point for the positive terminal of the current sense resistor used to measure and limit charge current.

**BATFET (Pin 22):** Gate control pin for a reverse blocking external N-channel MOSFET between the battery and $V_{OUT}$.

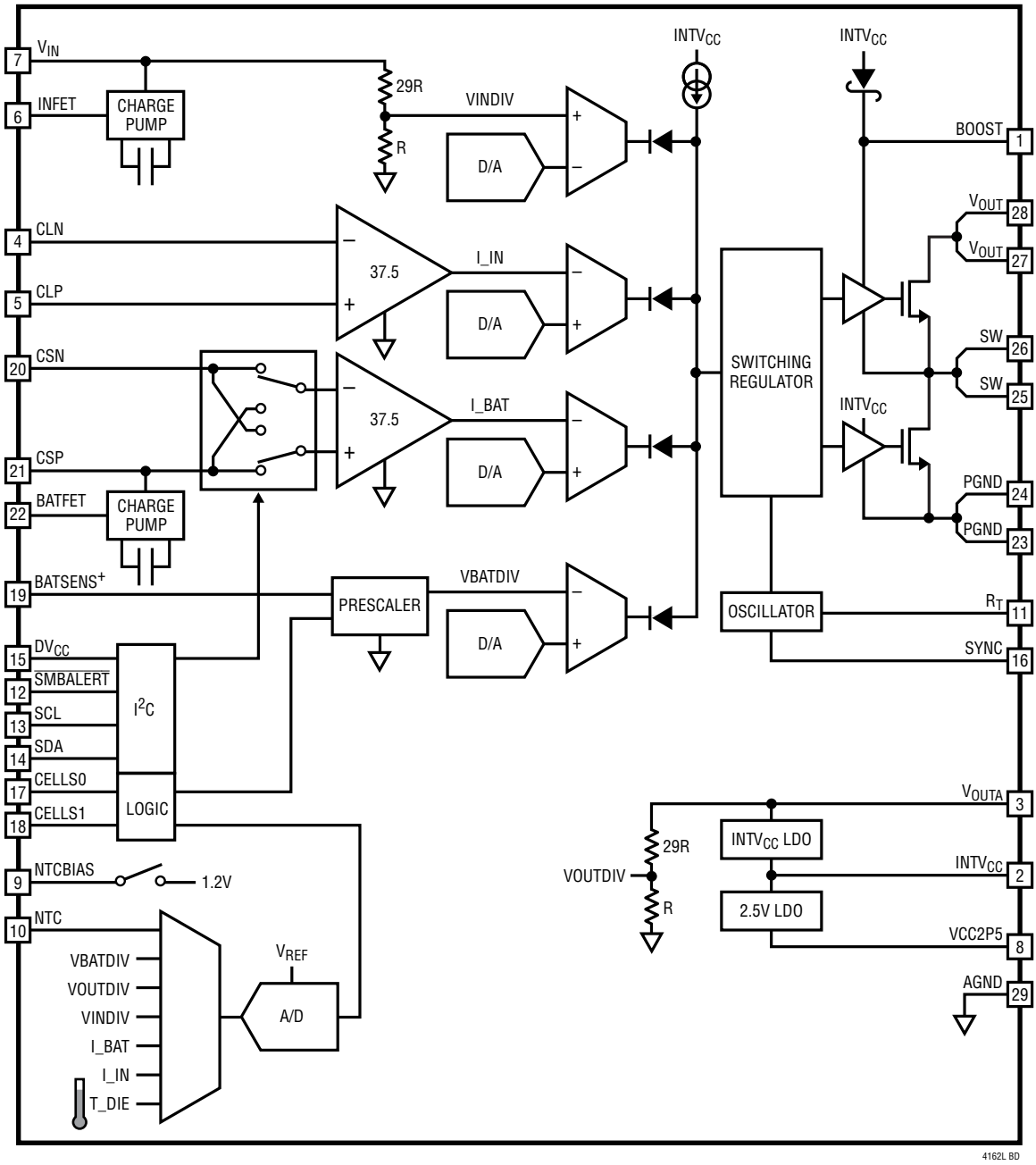
**PGND (Pins 23,24):** Power ground pins. These pins should be connected to a copper pour that forms the return for the $V_{OUT}$ bypass capacitor on the top layer of the printed circuit board.

**SW (Pin 25, 26):** Switching regulator power transmission pins. The SW pins deliver power from the $V_{OUT}$ pins to the battery via the step-down switching regulator. An inductor should be connected from SW to a sense resistor at CSP. See the Applications Information section for a discussion of inductor value and current rating.

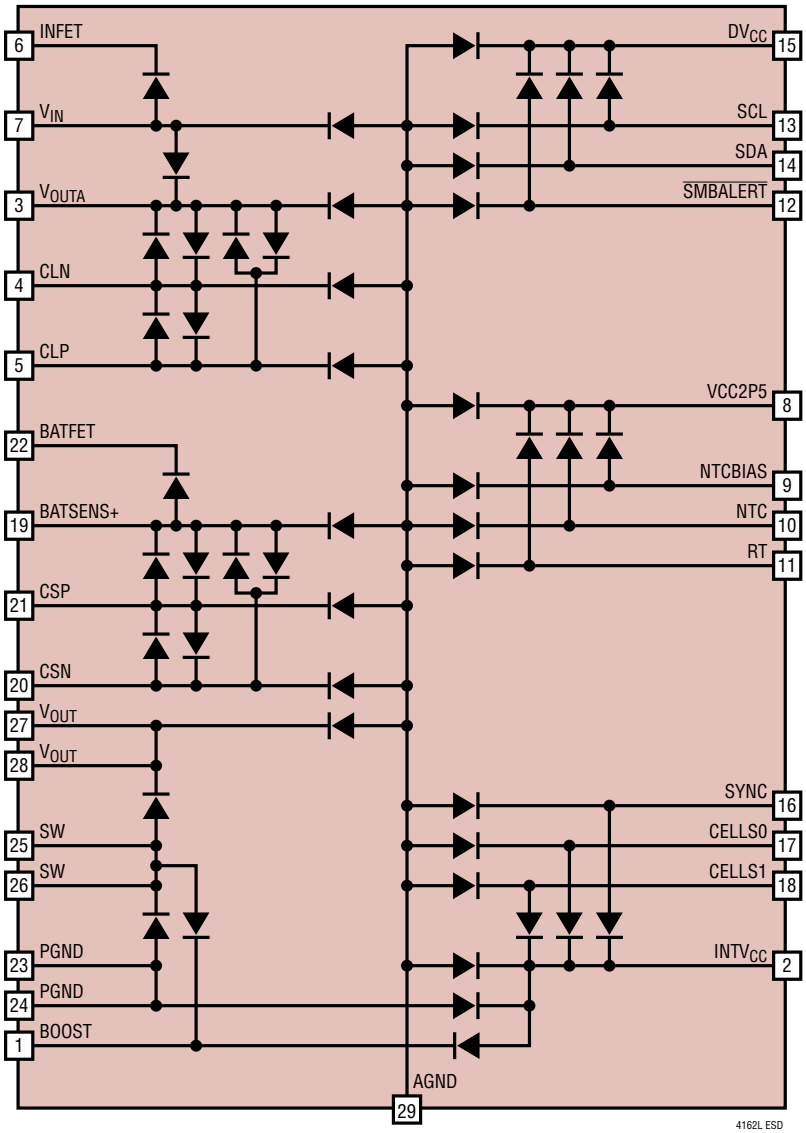
**$V_{OUT}$ (Pin 27, 28):** Switching regulator input pins. The $V_{OUT}$ pins deliver power to the switching charger. Having extremely high frequency current pulses, bypassing of the $V_{OUT}$ pins should take precedence over all other PCB layout considerations. A bypass capacitor of 10µF is a good starting point.

**AGND (Exposed PAD, Pin 29):** Analog ground pin. This is the ground pin used to return all of the analog circuitry inside the LTC4162 and should be connected to an analog ground pour that is common with PGND (pins 23 and 24). It should also be connected to a ground plane on layer 2 of the PCB to which all of the analog components return such as the $R_T$ resistor and the $INTV_{CC}$ and VCC2P5 bypass capacitors.

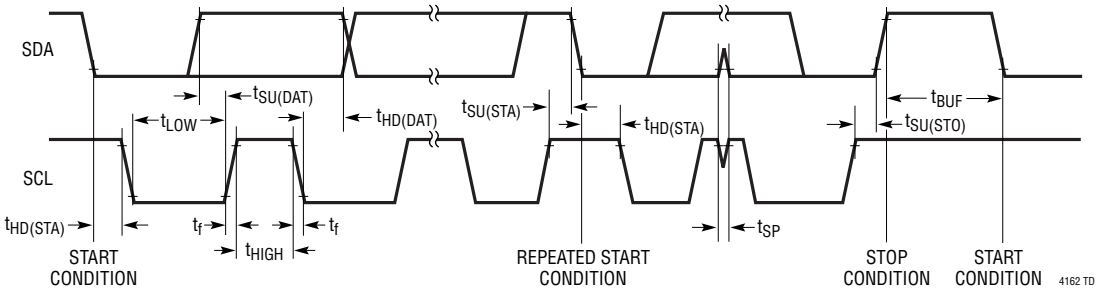
## BLOCK DIAGRAM



## ESD DIAGRAM


INFET
6
VIN
7
VOUTA
3
CLN
4
CLP
5
BATFET
22
BATSENS+
19
CSP
21
CSN
20
VOUT
27
VOUT
28
SW
25
SW
26
PGND
23
PGND
24
BOOST
1
AGND
29
DVCC
15
SCL
13
SDA
14
SMBALERT
12
VCC2P5
8
NTCBIAS
9
NTC
10
RT
11
SYNC
16
CELLS0
17
CELLS1
18
INTVCC
2
4162L ESD

# TIMING DIAGRAM




## I²C SMBus Legend

| | |
|---|---|
| S | START CONDITION |
| Sr | REPEATED START CONDITION |
| Rd | READ (BIT VALUE OF 1) |
| Wr | WRITE (BIT VALUE OF 0) |
| A | ACKNOWLEDGE |
| N | NACK |
| P | STOP CONDITION |
| PEC* | PACKET ERROR CODE |
| | MASTER TO SLAVE |
| | SLAVE TO MASTER |

### SMBus WRITE WORD PROTOCOL

| S | SLAVE ADDRESS | Wr | A | COMMAND CODE | A | DATA BYTE LOW | A | DATA BYTE HIGH | A | P |
|---|---|---|---|---|---|---|---|---|---|---|

### SMBus WRITE WORD WITH PEC PROTOCOL

| S | SLAVE ADDRESS | Wr | A | COMMAND CODE | A | DATA BYTE LOW | A | DATA BYTE HIGH | A | PEC* | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

### SMBus READ WORD PROTOCOL

| S | SLAVE ADDRESS | Wr | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | Rd | A | DATA BYTE LOW | A | DATA BYTE HIGH | N | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

### SMBus READ WORD WITH PEC PROTOCOL

| S | SLAVE ADDRESS | Wr | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | Rd | A | DATA BYTE LOW | A | DATA BYTE HIGH | A | PEC* | N | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

### SMBus ALERT RESPONSE ADDRESS PROTOCOL

| S | ALERT RESPONSE ADDRESS | Rd | A | DEVICE ADDRESS | Rd | N | P |
|---|---|---|---|---|---|---|---|

### SMBus ALERT RESPONSE ADDRESS PROTOCOL WITH PEC

| S | ALERT RESPONSE ADDRESS | Rd | A | DEVICE ADDRESS | Rd | A | PEC* | N | P |
|---|---|---|---|---|---|---|---|---|---|

*USE OF PACKET ERROR CHECKING IS OPTIONAL

# OPERATION

### Introduction

The LTC4162 is an advanced power manager and switching battery charger utilizing a high efficiency synchronous step-down switching regulator.

Using multiple feedback control signals, power is delivered from the input to the battery by a 1.5MHz constant-frequency step-down switching regulator. The switching regulator reduces output power in response to one of its four regulation loops including battery voltage, battery charge current, input current and input voltage.

The switching regulator is designed to efficiently transfer power from a variety of possible sources, such as USB ports, wall adapters and solar panels, to a battery while minimizing power dissipation and easing thermal budgeting constraints. Since a switching regulator conserves power, the LTC4162 allows the charge current to exceed the source's output current, making maximum use of the allowable power for battery charging without exceeding the source's delivery specifications. By incorporating input voltage and system current measurement and control systems, the switching charger ports seamlessly to these sources without requiring application software to monitor and adjust system loads. By decoupling the system load from the battery and prioritizing power to the system, the instant-on PowerPath architecture ensures that the system is powered upon input power arrival, even with a completely dead battery.

Two low power charge pumps drive external MOSFETs to provide low loss power paths from the input supply and battery to the system load while preventing the system node from back-driving the input supply or overcharging the battery. The power path from the battery to the system load guarantees that power is available to the system even if there is insufficient or absent power from $V_{IN}$. A wide range of input current settings as well as battery charge current settings are available by software control and by choosing the values of input and charge current sense resistors $R_{SNSI}$ and $R_{SNSB}$.

A measurement subsystem periodically monitors and reports on a large collection of system parameters via the $I^2C$ port. An interrupt subsystem can be enabled to alert the host microprocessor of various status change events so that system parameters can be varied as needed. All of the status change events are maskable for maximum flexibility. For example, features such as battery presence detection and battery impedance measurement are easily enabled.

To eliminate battery drain between manufacture and sale, a ship-and-store feature reduces the already low battery drain current even further.

The input undervoltage control loop can be engaged to keep the input voltage from decreasing beyond a minimum level when a resistive cable or power limited supply such as a solar panel is providing input power. A maximum power point tracking algorithm using this control loop can be deployed to maximize power extraction from solar panels and other resistive sources.

Finally, the LTC4162 has a digital subsystem that provides substantial adjustability so that power levels and status information can be controlled and monitored via the conventional $I^2C$ port.

### LTC4162 Digital System Overview

The LTC4162 contains an advanced digital system which can be accessed using the $I^2C$ port. Use of the $I^2C$ port is optional, it can be used extensively in the application or not at all, as dictated by the application requirements. Cell count, charge current, input current regulation and switching charger frequency are all externally configurable without using the $I^2C$ port. For applications requiring the LTC4162's advanced digital features, the $I^2C$ port provides a means to use status and A/D telemetry data from the measurement system, monitor charger operation, configure charger settings (e.g. charge voltage, charge current, temperature response, termination algorithm, etc), enable, disable, read and clear alerts, activate the low power ship mode, and enable/disable the battery charger.

### Power Path Controller

The LTC4162 features input and output N-channel MOSFET charge pump gate drivers. These drivers make up a dual unidirectional power path system that allows power to be delivered to the system load by either the input supply or the battery, whichever is greater. Only one of

## OPERATION

the external MOSFETs will be enabled at a time. If $V_{IN}$ is more than 150mV above BATSENS+, the MOSFET from the input to the system load will be enabled and the one from the system load to BATSENS+ will block conduction preventing overcharging of the battery. If $V_{IN}$ falls more than 20mV below BATSENS+ the MOSFET from the input supply to the system load will be disabled preventing reverse conduction and the MOSFET from BATSENS+ to the system load will be enabled powering downstream circuitry from the battery. It is important not to back drive $V_{OUT}$ as one or the other of the power path MOSFETs will always be enabled.

### Step Down Switching Battery Charger

The LTC4162's battery charger is based on a very efficient synchronous step down switching regulator. As with any modern battery charger, the LTC4162 incorporates both constant-current and constant-voltage feedback control loops to prevent overcharging. The switching charger can charge either a single cell or a battery of up to eight series Lithium-Ion/Polymer cells.

Normal charging begins with a constant current until the battery reaches its target voltage. The charge current is determined by the combination of the sense resistor, $R_{SNSB}$, placed in series with the inductor and the servo control voltage set by either icharge_jeita_2 through icharge_jeita_6 with en_jeita set or just charge_current_setting if en_jeita is cleared. An internal soft-start algorithm ramps up the charge current setting from zero to its present setting. Once the battery voltage reaches the programmed voltage limit the constant-current control loop hands off to the constant-voltage control loop. The final battery voltage is set with the combination of either vcharge_jeita_2 through vcharge_jeita_6 with en_jeita set or with just vcharge_setting if en_jeita is cleared. The cell_count, controlled by the CELLS0 and CELLS1 pins, is a charge voltage multiplier so that multiple series cells can be charged.

If en_jeita is set, the charge current is given by the expression:

$$I_{CHARGE} = (icharge_jeita_x + 1)\frac{1mV}{R_{SNSB}}$$

where icharge_jeita_2 through icharge_jeita_6 each range from 0 to 31.

If en_jeita is not set:

$$I_{CHARGE} = (charge_current_setting + 1)\frac{1mV}{R_{SNSB}}$$

where charge_current_setting ranges from 0 to 31.

If en_jeita is set, the charge voltage is given by the expression:

$V_{CHARGE}$ = (3.8125V + 12.5mV • vcharge_jeita_x) • cell_count

where vcharge_jeita_2 through vcharge_jeita_6 each range from 0 to 31.

If en_jeita is not set:

$V_{CHARGE}$ = (3.8125V + 12.5mV • vcharge_setting) • cell_count

where vcharge_setting ranges from 0 to 31.

Beyond the conventional constant-current and constant-voltage control loops, the LTC4162 also has the ability to monitor and control both input current and input voltage, regulating battery charge power based on any one of these four control loops. Power limit is prioritized based on the lowest set-point of the group. For example, if the combined system load plus battery charge current is large enough to cause the switching charger to reach the programmed input current limit, the input current limit will reduce charge current to limit the voltage across the input sense resistor, $R_{SNSI}$, to the iin_limit_target. Even if the charge current is programmed to exceed the allowable input current, the input current due to charge current will not be violated; the charger will reduce its current as needed. Similarly, the input voltage limit loop, controlled by input_undervoltage_setting, can be used to prevent resistive power sources such as a solar panel from dragging the input voltage down below its under-voltage lockout level.

Only target values can be programmed with the $I^2C$ port. The LTC4162 uses the target values as a starting point from which the charging algorithms calculate the actual values to be applied to the DACs to support functions such as

## OPERATION

temperature compensated charge voltages and currents, maximum power point tracking, charger soft starting, etc. The target value registers are read/write whereas the actual DAC value registers, icharge_dac, vcharge_dac, iin_limit_dac and input_undervoltage_dac are read only.

Due to its all NMOS switch design, a small charge pump capacitor is required from SW to BOOST to provide high side boosted drive for the top switch.

### Input Current Regulation

Input current control limits loading on the input source during periods of high system demand by sacrificing charge current. Note that the LTC4162 only has the authority to reduce charge current to zero and cannot further reduce input current below the system load current. The input current limit is controlled by a combination of the sense resistor, $R_{SNSI}$, from CLP to CLN and either the default 32mV servo voltage or a lower value set by iin_limit_target. The servo voltage across the sense resistor divided by the resistor's value determines the input current regulation set point. A 10mΩ resistor, for example, would have an upper input current limit of 3.2A using the default 32mV servo voltage. iin_limit_target has 6 bit resolution giving adjustable values from 500µV to 32mV in 500µV steps and can be calculated in Amperes, by the following expression:

$$I_{INLIM} = (iin_limit_target + 1)\frac{500\mu V}{R_{SNSI}}$$

where iin_limit_target ranges from integer values of 0 to 63.

### Input Undervoltage Regulation and Solar Panel Maximum Power Point Tracking (MPPT)

The LTC4162 also contains an undervoltage control loop that allows it to tolerate a resistive connection to the input power source by automatically reducing charge current as the $V_{IN}$ pin drops to input_undervoltage_setting. This circuit helps prevent UVLO oscillations by linearly regulating the input voltage above the LTC4162's undervoltage lockout level.

Optionally, the LTC4162 includes a maximum power point tracking (MPPT) algorithm to find and track the input_undervoltage_dac value that delivers the maximum charge current to the battery. If mppt_en is set, the MPPT algorithm performs a global sweep of input_undervoltage_dac values, measuring battery charge current at each setting. Once the sweep is complete, the LTC4162 applies the input_undervoltage_dac value corresponding to the maximum battery charge current ibat (i.e. the maximum power point). The LTC4162 then tracks small changes in the maximum power point by slowly dithering the input_undervoltage_dac. The LTC4162 performs a new global sweep of input_undervoltage_dac values every 15 minutes, applies the new maximum power point, and resumes dithering at that point. Alternatively, the global sweep will run immediately, bypassing the 15 minute wait, if ibat changes by more that 25%. With mppt_en, a solar panel can be used as a suitable power source for charging a battery and powering a load. The MPPT algorithm may not work for all solar panel applications and does not have to be used. Alternatively a solar panel can be used without the MPPT algorithm by setting the input_undervoltage_setting value to match the optimum loaded solar panel voltage, but significant shadows or drops in light will likely result in suboptimum power delivery.

Note that, due to the Power Path topology, current can flow from the input to the system load without being controlled by the LTC4162's switching charger. Therefore, the MPPT algorithm does not have full authority to track and find the maximum power point under all conditions. To obtain complete Maximum Power Point operation, it may be necessary to forgo the Power Path feature of the LTC4162 and connect the system load directly to the battery pack. In this configuration, the LTC4162 has full authority to track the maximum power point of the solar panel.

The input under voltage value, in Volts, will be given by the following expression:

$$V_{INLIM} = (input_undervoltage_setting + 1) \bullet 140.625mV$$

where input_undervoltage_setting ranges from integer values of 0 to 255.

# OPERATION

### System Controls

The switching battery charger can be disabled by setting suspend_charger. This might be necessary, for instance, to pass USB Suspend compliance testing. suspend_charger should be used with caution as a low battery situation could prevent the system processor from being able to clear it and may require a factory service call to remove and replace the battery.

### Input Overvoltage Protection

The LTC4162 has over-voltage detection on its input. If $V_{IN}$ exceeds approximately 38.6V as indicated by vin_ovlo, the switching charger will stop delivering power. The charger will resume switching if $V_{IN}$ falls below roughly 37.2V. The overvoltage detection cutoff circuit provides only modest over voltage protection and is not intended to prevent damage in all circumstances.

### Measurement Subsystem

The LTC4162 includes a 16-bit ΔΣ A/D converter and signal multiplexer to monitor numerous analog parameters. It can measure the voltages at vin, vbat and vout, the input current (voltage between CLP and CLN), iin, the battery charge current (voltage between CSP and CSN), ibat, the battery pack thermistor_voltage, its own internal die_temp and, once a charge cycle begins, the series resistance of the battery, bsr. To save battery current, the measurement system is disabled if the battery is the only source of power (vin_gt_vbat = 0). This can be overridden with force_telemetry_on. The A/D converter is automatically multiplexed between all of the measured channels and its 16-bit signed two's complement results are stored in registers accessible via the $I^2C$ port. The seven channels measured by the ADC each take approximately 1.6ms to convert. The maximum range of the 16 bit ΔΣ A/D converter is ±1.8V and it has an internal span term of 18191 counts per Volt. It measures each of the above parameters through different paths giving different sensitivity terms for each measurement as summarized in Table 1.

### Battery Voltage Measurement

Battery voltage is measured through a resistive voltage divider whose attenuation ratio is based on the cell_count. The result is reported in vbat. The divider ratio is BATSENS+/(3.5 • cell_count) making the A/D span term 3.5 • cell_count/18191 or 192.4µV • cell_count per LSB where cell_count varies from 1 to 8. An alert may be set on battery voltage by setting the vbat based value vbat_lo_alert_limit or vbat_hi_alert_limit and setting en_vbat_lo_alert or en_vbat_hi_alert. These alerts are indicated by vbat_lo_alert or vbat_hi_alert and are cleared by writing them to 0.

### Input Voltage Measurement

Input voltage is measured through a 30:1 resistive voltage divider making the A/D span term for input voltage measurements 30/18191 or 1.649mV/LSB and is digitized to vin. An alert may be set on input voltage by setting the value vin_lo_alert_limit or vin_hi_alert_limit and setting en_vin_lo_alert or en_vin_hi_alert. These alerts are indicated by vin_lo_alert and vin_hi_alert and are cleared by writing them to 0.

**Table 1. Measurement Subsystem LSB Sizes**

| MEASUREMENT | UNITS | REGISTER SYMBOL | LSB SIZE | OFFSET |
|---|---|---|---|---|
| BATTERY VOLTAGE | V | vbat | 192.4µV • cell_count | |
| INPUT VOLTAGE | V | vin | 1.649mV | |
| OUTPUT VOLTAGE | V | vout | 1.653mV | |
| INPUT CURRENT | A | iin | 1.466µV/RSNSI | |
| BATTERY CURRENT | A | ibat | 1.466µV/RSNSB | |
| DIE TEMPERATURE | °C | die_temp | 0.0215°C | 264.4°C |
| BATTERY IMPEDANCE | Ω | bsr | RSNSB • cell_count/500 | |
| THERMISTOR VOLTAGE | V | thermistor_voltage | 45.833µV/V | |

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### $V_{OUT}$ Voltage Measurement

Output voltage is measured through a 30.07:1 resistive voltage divider making the A/D span term for output voltage measurements 30.07/18191 or 1.653mV/LSB and is digitized to vout. An alert may be set on output voltage by setting the value vout_lo_alert_limit or vout_hi_alert_limit and setting en_vout_lo_alert or en_vout_hi_alert. These alerts are indicated by vout_lo_alert and vout_hi_alert and are cleared by writing them to 0.

### Battery Current Measurement

Battery current is measured with a current sense resistor between the CSP and CSN pins. An amplifier with a gain of 37.5 amplifies this signal and refers it to ground internally so that the A/D converter can measure it. The sensed battery current is therefore given by $I_{BAT} \bullet R_{SNSB} \bullet 37.5$. For a 10mΩ $R_{SNSB}$ current sense resistor, the A/D sensitivity is 1/(18191 • 10mΩ • 37.5) or 146.6µA/LSB. The battery current measurement system has a built in commutator. While charging a battery, two's complement number ibat will be positive representing current into the battery. When the battery charger is disabled or terminated, as detected by charger_suspended, the commutator is activated and ibat will be negative, representing current out of the battery. An alert may be set on the ibat measurement by setting the desired value in ibat_lo_alert_limit and setting en_ibat_lo_alert. While charging, ibat_lo_alert_limit can be used to detect when the charge current has dropped below a given threshold. When charger_suspended, if set to a negative number, ibat_lo_alert_limit can be used to detect if the battery load has exceeded a given threshold. This alert is indicated by ibat_lo_alert and is cleared by writing it to 0.

### Input Current Measurement

Input current is measured with a current sense resistor between the CLP and CLN pins. An amplifier with a gain of 37.5 amplifies this signal and refers it to ground internally so that the A/D converter can measure it. The sensed input current is therefore given by $I_{IN} \bullet R_{SNSI} \bullet 37.5$. For a 10mΩ $R_{SNSI}$ current sense resistor, the A/D sensitivity is 1/(18191 • 10mΩ • 37.5) or 146.6µA/LSB. The input current is digitized to iin. An upper limit alert may be set on input current by setting the value iin_hi_alert_limit and setting the en_iin_hi_alert. This alert is indicated by iin_hi_alert and is cleared by writing it to 0.

### Battery Series Resistance (BSR) Measurement

The LTC4162 can optionally measure the series resistance of the battery stack or cell. If run_bsr is set, the LTC4162 momentarily suspends the battery charger and calculates the battery series resistance by dividing the voltage change (charging vs not charging) by the measured charge current (bsr_charge_current).

The per-cell resistance value is reported in bsr and the charge current observed during the measurement is reported in bsr_charge_current. The LTC4162 automatically resets run_bsr after the bsr measurement is complete. The total battery series resistance value is proportional to the charge current sense resistor, $R_{SNSB}$, as well as the cell_count, and can be computed in Ω from the expression:

$$R_{BAT}(\Omega) = \frac{bsr \bullet cell_count \bullet R_{SNSB}}{500}$$

Higher bsr_charge_current during a bsr measurement results in a more accurate bsr measurement. Very low values of bsr_charge_current may adversely impact the accuracy of the bsr measurement. If charge current is less than C/10 (bsr_charge_current < icharge_over_10), bsr_questionable will be set indicating that bsr_charge_current during the bsr test was less than optimum for an accurate reading. Recall that full charge current typically flows at the beginning of a charge cycle (presuming the battery is more deeply depleted) and will diminish when the charger enters the constant voltage phase of charging.

If run_bsr is set to 1 and the battery charger is not currently running, then the LTC4162 will be queued to perform the bsr measurement only after the start of the next charge cycle. An alert can be set with en_bsr_done_alert to generate a bsr_done_alert indicating that a bsr measurement is complete and that the result is available. A bsr_hi_alert may also be set on battery series impedance by writing a bsr_hi_alert_limit and setting en_bsr_hi_alert. Again, the bsr reading is the per-cell battery resistance and should be scaled by cell_count or, consequently, the target total re-

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sistance threshold for bsr_hi_alert_limit should be divided by cell_count before being written to bsr_hi_alert_limit.

bsr_done_alert and bsr_hi_alert are cleared by writing them to 0.

### Die Temperature Measurement

The LTC4162 has an integrated die temperature sensor that is monitored by the A/D converter and is digitized to die_temp. The die temperature is derived from an internal circuit and follows the equation:

$$T_{DIE}(°C) = die_temp \bullet 0.0215°C/LSB - 264.4°C$$

An alert may be set on die temperature by setting the value die_temp_hi_alert_limit and setting en_die_temp_hi_alert. This alert is indicated by die_temp_hi_alert and is cleared by writing it to 0.

To set the die_temp_hi_alert_limit, compute the threshold value from:

$$die_temp_hi_alert_limit = \frac{T_{DIE}(°C) + 264.4°C}{0.0215°C/LSB}$$

### Battery Temperature (NTC Thermistor) Measurement

To measure the battery temperature using a thermistor, connect the thermistor, $R_{NTC}$, normally being located in the battery pack, between the NTC pin and ground, and a low drift bias resistor, $R_{NTCBIAS}$, between NTCBIAS and NTC. $R_{NTCBIAS}$ should be a 1% or better resistor with a value equal to the value of the chosen thermistor at 25°C (R25). The LTC4162 applies an excitation voltage of 1.2V to $R_{NTCBIAS}$ to measure the thermistor value. The thermistor measurement result is available at thermistor_voltage. To minimize battery stress due to charging at temperature extremes, the LTC4162 has both a simple and a more advanced JEITA (Japan Electronics and Information Technology Industries Association) temperature qualified charging algorithm. If the application does not require temperature controlled charging, then the thermistor should be replaced with a resistor of equal value to the bias resistor $R_{NTCBIAS}$ to continuously simulate 25°C. If the thermistor is found to be open (thermistor_voltage > open_thermistor) either during the battery detection test or during charging, charger_state will switch to bat_missing_fault and charging will halt. Either a thermistor_voltage_lo_alert or thermistor_voltage_hi_alert may be set with en_thermistor_voltage_lo_alert or en_thermistor_voltage_hi_alert, both of which are cleared by writing them to 0.

The temperature vs resistance curve of a thermistor can be obtained from thermistor manufacturers in either table form or estimated by applying the modified Steinhart-Hart equation:

$$R_{NTC} = R_{25} \bullet e^{\left(A + \frac{B}{T_C + 273.15} + \frac{C}{(T_C + 273.15)^2} + \frac{D}{(T_C + 273.15)^3}\right)}$$

Where $R_{25}$ is the thermistor's resistance at 25°C and A, B, C and D are provided by the thermistor manufacturer and $T_C$ is the temperature in °C.

The temperature of the thermistor is computed from its resistance value by the complementary Steinhart-Hart expression where A1, B1, C1 and D1 are also provided by the thermistor manufacturer.

$$T_C = \frac{1}{A_1 + B_1 \ln\left(\frac{R_{NTC}}{R_{25}}\right) + C_1 \ln^2\left(\frac{R_{NTC}}{R_{25}}\right) + D_1 \ln^3\left(\frac{R_{NTC}}{R_{25}}\right)} - 273.15^oC \quad (1)$$

Alternatively, the more common but less accurate condensed version of Steinhart-Hart using the ubiquitous β parameter may be employed:

$$R_{NTC} = R_{25} \bullet e^{-\beta_{25/85}\left(\frac{1}{298.15^oC} - \frac{1}{T_C + 273.15^oC}\right)}$$

Where again, $R_{25}$ is the thermistor's resistance at 25°C and several β values are provided by the thermistor manufacturer, one for each of a number of temperature ranges.

The inverse β form is:

$$T_C = \frac{\beta_{25/85}}{\ln\left(\frac{R_{NTC}}{R_{25}}\right) + \frac{\beta_{25/85}}{298.15^oC}} - 273.15^oC \quad (2)$$

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The LTC4162 thermistor measurement system is designed specifically for a thermistor with a $\beta_{25/85}$ value of 3490K and returns thermistor_voltage where:

$$thermistor_voltage = 18191 \bullet 1.2 \bullet \frac{R_{NTC}}{R_{NTC}+R_{NTCBIAS}}$$

where typically $R_{NTCBIAS}$ is set equal to $R_{25}$, the 25°C value of the thermistor. To arrive at the thermistor's temperature in °C from thermistor_voltage substitute $R_{NTC}$ from:

$$R_{NTC} = R_{NTCBIAS} \bullet \frac{thermistor_voltage}{18191 \bullet 1.2 - thermistor_voltage}$$

into Equation 1 or Equation 2.

For thermistors with a $\beta_{25/85}$ value higher than 3490K see Alternate Thermistors and Biasing in the Applications Information section.

### Output Current Measurement

There is no sense resistor dedicated to measuring output current but its value can be obtained nonetheless. Output current is delivered from the input supply if vin_gt_vbat is true and from the battery if it is false.

If vin_gt_vbat is true and the battery charger is enabled (en_chg is true) then the input current measurement will be the sum of current to the switching charger and the output load. In this instance the switching charger will need to be disabled with suspend_charger to obtain an output current reading. It's also possible that the charger may already be terminated. If en_chg is false then set telemetry_speed to tel_high_speed, wait 20ms or more, and record iin as output current. If en_chg is true then set both suspend_charger and force_telemetry_on to 1 and telemetry_speed to tel_high_speed, wait 20ms or more for at least one telemetry cycle, and again record iin as output current. suspend_charger should then be cleared. Note that suspending the charger resets the tchargetimer and tcvtimer termination timers to 0.

On the other hand if vin_gt_vbat is false then the output current will be delivered from the battery and its value can be obtained from –ibat. Since vin_gt_vbat is low, the telemetry system will be disabled and the ibat reading will be stale. To enable the telemetry system, set force_telemetry_on to 1 and telemetry_speed to tel_high_speed. telemetry_valid indicates when fresh telemetry readings are available. To avoid polling for telemetry_valid a telemetry_valid_alert can be set with en_telemetry_valid_alert. Once the reading is obtained, force_telemetry_on can be cleared or telemetry_speed set to tel_low_speed for power savings.

### Low Power Telemetry

If input power is available (vin_gt_vbat = 1), and the battery is being charged, the telemetry system will be in its high speed mode returning results at a rate of roughly once per 11ms. If, on the other hand, charging has terminated normally or paused due to battery temperature out of range, the telemetry system will drop back to a rate of about once every 5 seconds to save power. When input power is not available (vin_gt_vbat = 0) it is still possible to collect telemetry data by setting force_telemetry_on. To save power in this mode the telemetry system will default to the lower speed 5 second mode. To force the higher telemetry rate, and suffer the higher quiescent current of roughly 2.5mA, the telemetry_speed can be set to the higher ~11ms rate by setting it to tel_high_speed.

### Configurable Limit Alert Subsystem

The $I^2C$ port also supports the SMBus $\overline{SMBALERT}$ protocol, including the Alert Response Address. An alert can optionally be generated if a monitored parameter exceeds a programmed limit or if a selected battery charger_state or any of a wide number of other charge_status change or fault events occur. This off-loads much of the continuous monitoring from the system's microcontroller and onto the LTC4162; reducing bus traffic and microprocessor load.

The $\overline{SMBALERT}$ pin is asserted (pulled low) whenever an enabled alert occurs. After asserting an interrupt, the LTC4162 responds to the host's Alert Response Address (ARA = 0b0001100[1]) with its own read address. If another part with a pending alert and a lower address also responds, that part wins the arbitration and the LTC4162 will stop responding to this ARA, keeping its $\overline{SMBALERT}$ pin asserted. Only a response of the LTC4162's complete read address will clear the LTC4162's $\overline{SMBALERT}$ signal. This allows the system to have many parts share a common interrupt line. If multiple parts are asserting the $\overline{SMBALERT}$

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**Table 2. Summary of Limit Alerts Registers**

| ALERT VALUE SETTING (0x01 – 0x0C) | EN_LIMIT_ALERTS_REG | LIMIT_ALERTS_REG |
|---|---|---|
| vin_hi_alert_limit | en_vin_hi_alert | vin_hi_alert |
| vin_lo_alert_limit | en_vin_lo_alert | vin_lo_alert |
| thermistor_voltage_hi_alert_limit | en_thermistor_voltage_hi_alert | thermistor_voltage_hi_alert |
| thermistor_voltage_lo_alert_limit | en_thermistor_voltage_lo_alert | thermistor_voltage_lo_alert |
| bsr_hi_alert_limit | en_bsr_hi_alert | bsr_hi_alert |
| die_temp_hi_alert_limit | en_die_temp_hi_alert | die_temp_hi_alert |
| ibat_lo_alert_limit | en_ibat_lo_alert | ibat_lo_alert |
| iin_hi_alert_limit | en_iin_hi_alert | iin_hi_alert |
| vout_hi_alert_limit | en_vout_hi_alert | vout_hi_alert |
| vout_lo_alert_limit | en_vout_lo_alert | vout_lo_alert |
| vbat_hi_alert_limit | en_vbat_hi_alert | vbat_hi_alert |
| vbat_lo_alert_limit | en_vbat_lo_alert | vbat_lo_alert |
| NA | en_bsr_done_alert | bsr_done_alert |
| NA | en_telemetry_valid_alert | telemetry_valid_alert |

**Table 3. Summary of Charger State Alerts**

| CHARGER_STATE_REG | EN_CHARGER_STATE_ALERTS_REG | CHARGER_STATE_ALERTS_REG |
|---|---|---|
| bat_detect_failed_fault | en_bat_detect_failed_fault_alert | bat_detect_failed_fault_alert |
| battery_detection | en_battery_detection_alert | battery_detection_alert |
| charger_suspended | en_charger_suspended_alert | charger_suspended_alert |
| precharge | en_precharge_alert | precharge_alert |
| cc_cv_charge | en_cc_cv_charge_alert | cc_cv_charge_alert |
| ntc_pause | en_ntc_pause_alert | ntc_pause_alert |
| timer_term | en_timer_term_alert | timer_term_alert |
| c_over_x_term | en_c_over_x_term_alert | c_over_x_term_alert |
| max_charge_time_fault | en_max_charge_time_alert | max_charge_time_fault_alert |
| bat_missing_fault | en_bat_missing_fault_alert | bat_missing_fault_alert |
| bat_short_fault | en_bat_short_fault_alert | bat_short_fault_alert |

**Table 4. Summary of Charger Status Alerts**

| CHARGE_STATUS_REG | EN_CHARGE_STATUS_ALERTS_REG | CHARGE_STATUS_ALERTS_REG |
|---|---|---|
| constant_voltage | en_constant_voltage_alert | constant_voltage_alert |
| constant_current | en_constant_current_alert | constant_current_alert |
| iin_limit_active | en_iin_limit_active_alert | iin_limit_active_alert |
| vin_uvcl_active | en_vin_uvcl_active_alert | vin_uvcl_active_alert |
| thermal_reg_active | en_thermal_reg_active_alert | thermal_reg_active_alert |
| ilim_reg_active | en_ilim_reg_active_alert | ilim_reg_active_alert |

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signal then multiple reads from the ARA are needed. For more information refer to the SMBus specification.

After the ARA process is complete, alert bits can be cleared by individually writing them to 0 and writing the remaining bits in the register to 1. This preserves any other pending alert bits as writing 1s to the alert registers are ignored.

### Series Cell Count Selection

Cell count selection of up to eight series cells is made via the CELLS1 and CELLS0 pins. CELLS1 and CELLS0 should be pin strapped to either GND, VCC2P5, or $INTV_{CC}$ to make the cell_count selection (see Table 5). For added safety, cell_count can be read back from the $I^2C$ port. The GND/GND combination will result in a cell_count_err and will inhibit charging. Note that the number of cells multiplied by their expected maximum cell voltage during charging cannot exceed $V_{IN} – V_{IN_DUVLO}$.

**Table 5. CELLS0 and CELLS1 Pin Mapping to Series Cell Count**

| CELLS1 | CELLS0 | cell_count |
|---|---|---|
| $INTV_{CC}$ | $INTV_{CC}$ | 1 |
| $INTV_{CC}$ | VCC2P5 | 2 |
| $INTV_{CC}$ | GND | 3 |
| VCC2P5 | $INTV_{CC}$ | 4 |
| VCC2P5 | VCC2P5 | 5 |
| VCC2P5 | GND | 6 |
| GND | $INTV_{CC}$ | 7 |
| GND | VCC2P5 | 8 |

When charging stacks of two or more cells in series it is important to consult with the battery manufacturer to ascertain requirements pertaining to cell balancing. Repeatedly charging series stacks of cells without balancing is usually degenerative and typically leads to increased mismatch accompanied with shorter battery life. For high reliability applications an auxiliary battery balancer is recommended.

### Battery Detection

The LTC4162 begins a charging cycle by performing a 2-4 second battery detection test, during which a 1mA load is drawn from the battery followed by a small charge current being sent to the battery. If the battery voltage remains stable during the battery detection test, the LTC4162 proceeds with battery charger soft-start. If the battery voltage does not remain stable, the LTC4162 proceeds with a battery open/short test. The battery is charged at minimum charge current for one to two seconds. Abnormal results from the battery detection test result in charger_state becoming bat_missing_fault, bat_short_fault or bat_detect_failed_fault and will prevent further charging. A charger_state of bat_missing_fault will also occur if the thermistor is open or has a very high value (thermistor_voltage > open_thermistor). Programmable interrupts en_bat_short_fault_alert, en_bat_missing_fault_alert and en_bat_detect_failed_fault_alert can be set to generate an $\overline{SMBALERT}$ if one of these cases occurs. In the event of a battery detection fault, the battery detection test will retry every 30 seconds.

### Battery Charger Soft-Start

The LTC4162 soft starts charge current by ramping icharge_dac from 0 to its target charge current setting at a nominal rate of 400µS per icharge_dac LSB. This results in a maximum charge current soft start time of 31 • 400µs or 12.4ms. Any time the battery charger needs to change its charge current setting up or down, the ramp routine is invoked. The charge current target is derived from either charge_current_setting or the JEITA temperature qualified charging system, icharge_jeita_2 through icharge_jeita_6 (See Advanced JEITA Temperature Controlled Charging).

### Low Battery

When a charge cycle begins, The LTC4162 first determines if the battery is deeply discharged. If the BATSENS+ pin voltage is lower than about 2.5V, the battery charger delivers roughly 10mA directly from $INTV_{CC}$. This operating mode is mainly used to pull a pack protected battery out of protection mode. When the BATSENS+ pin voltage reaches 2.5V, charging hands over to the switching battery charger. Above 2.5V absolute level but below about 2.85V per cell_count the LTC4162 applies a preconditioning charge setting equal to approximately C/10 (icharge_dac = 3), and reports precharge. When the battery voltage exceeds 2.85V per cell_count, the LTC4162 proceeds to the full constant-current/constant-voltage charging phase and reports cc_cv_charge.

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### Constant-Current Charging

When the battery voltage is above 2.85V per cell_count, the charger will attempt to deliver either (icharge_jeita_x + 1) • 1mV/$R_{SNSB}$ with en_jeita or (charge_current_setting + 1) • 1mV/$R_{SNSB}$ without en_jeita in constant-current mode where icharge_jeita_x or charge_current_setting ranges from 0 to 31. For example, A 10mΩ resistor between CPS and CSN would give an upper limit charge current of 3.2A. Depending on available input power and external load conditions, the battery charger may not be able to charge at the full programmed rate. An alternate control loop such as the input current limit loop or input voltage limit loop may be in force and only partial power will be available to charge the battery. If input current limit is reached, for instance, the system load will be prioritized over the battery charge current. When system loads are light, battery charge current will be maximized and could be as high as the value programmed by icharge_jeita_x or charge_current_setting.

The charge current programming resistor, $R_{SNSB}$, should always be set to match the capacity of the battery without regard to source or load limitations from any other control loop. The multiple control-loop architecture of the LTC4162 will correct for any discrepancies, always optimizing transfer of power to the battery and the load.

### Thermal Regulation

When the switching battery charger is enabled at an elevated ambient temperature, LTC4162 self heating may push its junction temperature to an unacceptable level. To prevent overheating the LTC4162 monitors its own die_temp and automatically reduces the icharge_dac to limit power dissipation. The differential servo voltage at CSP to CSN can drop to as low as 1mV giving about 3% (1/32) of the maximum charge current. The thermal regulation algorithm achieves this by enforcing a maximum icharge_dac setting which drops linearly from 31 to 0 as die_temp increases from thermal_reg_start_temp (default 120°C) to thermal_reg_end_temp (default 125°C). When the thermal regulation algorithm is active, charge_status becomes thermal_reg_active. A thermal_reg_active_alert can be set with en_thermal_reg_active_alert and cleared by writing either back to 0. Thermal regulation can be programmed to any temperature within the LTC4162's operating range.

### Constant-Voltage Charging

Once the BATSENS+ voltage reaches the programmed charging voltage the switching regulator will reduce its output power and hold the battery voltage steady at either (3.8125V + 12.5mV • vcharge_jeita_x) • cell_count with en_jeita or (3.8125V + 12.5mV • vcharge_setting) • cell_count without en_jeita where vcharge_jeita_x and vcharge_setting each range from 0 to 31. In constant voltage mode the charge current will decrease naturally toward zero providing inherently safe operation by preventing the battery from being over charged. Multiple charge voltage settings are available for final top-off voltage selection via vcharge_jeita_x with en_jeita or vcharge_setting without en_jeita. While charge voltage trade-offs can be made to preserve battery life or maximize capacity, it is not possible for the LTC4162 to be set to a charge voltage that is dangerously high or inconsistent with a Lithium-Ion/Polymer Battery.

Note that charge_current_setting and vcharge_setting do not directly control the icharge_dac and vcharge_dac. They are only target values. For example, if the JEITA Temperature Controlled Charging system is enabled (en_jeita = 1), the DACs will be controlled by this user programmable system (i.e. icharge_jeita_2 through icharge_jeita_6, vcharge_jeita_2 through vcharge_jeita_6).

### Basic Temperature Controlled Charging

The LTC4162 provides temperature controlled charging if a grounded thermistor and a bias resistor are connected to the NTCBIAS and NTC pins and en_jeita is set to 0. Charging is paused if thermistor_voltage rises above jeita_t1 (0°C) or falls below jeita_t6 (60°C). Recall that thermistors have a negative temperature coefficient so higher temperatures will read lower thermistor_voltage and vice versa. If charging is not suspended, the charging voltage and current will follow vcharge_setting and charge_current_setting respectively.

The default upper and lower limits are based on a thermistor with a $\beta_{25/85}$ value of 3490K, such as provided by a Vishay NTCS0402E3103FLT. This thermistor was chosen

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specifically because of its weak temperature characteristic relative to other thermistors. Stronger thermistors can be diluted to match it by placing a low drift resistor in series with the thermistor and increasing the bias resistor accordingly. (see Alternate Thermistors and Biasing in Applications Information for details). If the application does not require temperature controlled charging then the thermistor should be replaced with a resistor of equal value to bias resistor $R_{NTCBIAS}$, for example, 100kΩ.

### Advanced JEITA Temperature Controlled Charging

A control system is included to provide compliance with the Japan Electronics and Information Technology Industries Association guidelines on battery charging by leaving en_jeita set to its default value of 1. Specifically, a very flexible multi-point temperature-voltage-current profile can be programmed into the LTC4162 to ensure that charging parameters as a function of temperature are used. Figure 1 and Table 6 illustrate default values of the JEITA system available in the LTC4162. There are seven distinct temperature regions programmed by the six thermistor_voltage based temperature set points jeita_t1 through jeita_t6. For each of the temperature regions, the charge current and charge voltage can be programmed within the limits set by $(V_{CSP} - V_{CSN})/R_{SNSB}$ (charge_current_setting) and battery charge voltage (vcharge_setting). When en_jeita is true, The JEITA system writes its registers, icharge_jeita_2 through icharge_jeita_6 and vcharge_jeita_2 through vcharge_jeita_6 to charge_current_setting and vcharge_setting which are then passed on to the icharge_dac and vcharge_dac.

*Writing values to* charge_current_setting *and* vcharge_setting *with* en_jeita *set is futile as the JEITA system will overwrite these values every 11ms.*

The values for the JEITA registers are shown below. The bold values in the tables are programmable. The jeita_t1 through jeita_t6 registers determine the thermistor_voltage values for the breakpoints between regions. Table 6 lists the default values of the JEITA charging parameters along with example values of a 10kΩ thermistor with a β value of 3490K. All of the temperature, voltage and current settings can be modified for maximum flexibility.

**Table 6. Tabular Representation of the JEITA system, Default JEITA Values and β = 3490K Equivalent Temperatures**

| jeita_region | vcharge_jeita | Charge Voltage | icharge_jeita | Charge Current | JEITA Temperature | thermistor_voltage | RNTC | Temp |
|---|---|---|---|---|---|---|---|---|
| R1 | Charger Off | | | | | | | |
| | | | | | jeita_t1 | **16117** | 28215Ω | 0°C |
| R2 | **31** | 4.20V | **15** | 16mV/$R_{SNSB}$ | | | | |
| | | | | | jeita_t2 | **14113** | 18290Ω | 10°C |
| R3 | **31** | 4.20V | **31** | 32mV/$R_{SNSB}$ | | | | |
| | | | | | jeita_t3 | **7970** | 5751Ω | 40°C |
| R4 | **23** | 4.10V | **31** | 32mV/$R_{SNSB}$ | | | | |
| | | | | | jeita_t4 | **7112** | 4832Ω | 45°C |
| R5 | **23** | 4.10V | **15** | 16mV/$R_{SNSB}$ | | | | |
| | | | | | jeita_t5 | **6325** | 4080Ω | 50°C |
| R6 | **19** | 4.05V | **15** | 16mV/$R_{SNSB}$ | | | | |
| | | | | | jeita_t6 | **4970** | 2948Ω | 60°C |
| R7 | Charger Off | | | | | | | |

Rev A

## OPERATION

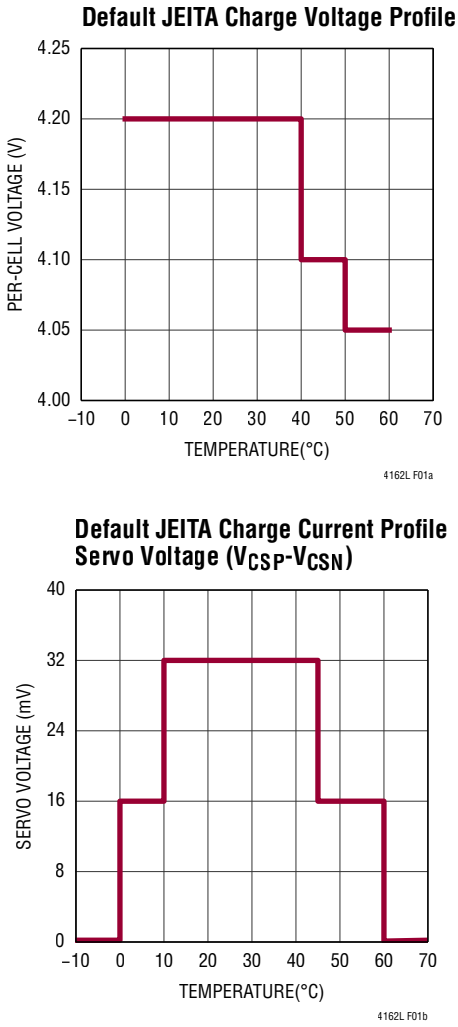


**Figure 1. Default JEITA Temperature Profile Gives A Graphical Representation of the Seven JEITA Regions, the Six Breakpoint and the Default Values**

### Battery Charger Termination and Full Charge Indication (C/x)

The LTC4162 supports several battery charge termination methods.

If enabled, a maximum elapsed charge time timer is started at the beginning of each charge cycle and, upon achieving constant_voltage regulation, a constant-voltage timer is also started. At the expiration of either of these timers, charging of the battery will discontinue and no more current will be delivered. The elapsed time timer expires when tchargetimer reaches max_charge_time and the constant-voltage timer expires in constant_voltage when tcvtimer reaches max_cv_time. Default max_cv_time is 14400 seconds (4 hours). To set different timer expiration values, max_charge_time and max_cv_time are both adjustable. The resolution of max_cv_time is 1 second/LSB and for max_charge_time it is 1 minute/LSB.

tcvtimer can be read back to determine the cummulative time in constant_voltage regulation. max_cv_time is a 16 bit unsigned value ranging from 0 to 65535 seconds (~18 hours). tchargetimer, the total charge time safety timer, can be read back at any time to determine the elapsed time since the beginning of this charge cycle. max_charge_time is a 16 bit unsigned value at 1 minute per LSB ranging from 0 to 65535 minutes (~45 days). The tchargetimer is disabled when max_charge_time is left at its default value of 0. To enable the tchargetimer write a non 0 value to max_charge_time.

max_charge_time_fault indicates that charging has terminated due to tchargetimer reaching max_charge_time and timer_term indicates that charging has terminated due to tcvtimer reaching max_cv_time. The max_charge_time_fault will persist until either the battery voltage drops to less than 35% of its target voltage setting, whereupon a new charge cycle begins and the tchargetimer resets, or a power cycle occurs resetting the entire charger state machine. A normal termination such as timer_term or c_over_x_term also resets tchargetimer. Finally, the max_charge_time_fault is cleared upon abnormal conditions such as the input voltage falling below the BATSENS+ pin voltage, suspend_charger or if any another system fault occurs: not intvcc_gt_2p8v, not vin_gt_4p2v, not vin_gt_vbat, thermal_shutdown, no_rt or cell_count_err.

Alternately, if en_c_over_x_term is set, the LTC4162 will also terminate charging once constant_voltage is reached and ibat has naturally dropped to the c_over_x_threshold. The default c_over_x_threshold value of c_over_10 is a good indication that the battery has reached a nearly full state of charge. The c_over_x_threshold is adjustable via the $I^2C$ port. If en_c_over_x_term is set, charging will terminate at the first of either c_over_x_term, timer_term or max_charge_time_fault. The constant_voltage timer

## OPERATION

termination features cannot be disabled. Both of the charge timers will be paused in ntc_pause.

The LTC4162 can optionally be configured to generate an interrupt at C/x termination by setting en_c_over_x_term_alert. Timer termination alerts can also be set with either en_timer_term_alert for the constant_voltage timer or en_max_charge_time_alert for max_charge_time_fault.

c_over_x_term, timer_term and max_charge_time_fault determine what caused the $\overline{\text{SMBALERT}}$. The LTC4162 terminates charging by disabling the switching charger which makes the SW node high impedance.

### Automatic Recharge

After a normal termination, the charger will remain off. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a new charge cycle will automatically begin when the battery voltage falls below approximately 97.5% of the programmed charge voltage. The termination safety timers, tcvtimer and tchargetimer, will reset back to zero. A new charge cycle will also be initiated if input power is cycled or if the charger is momentarily disabled (e.g. suspend_charger set to 1, then back to 0).

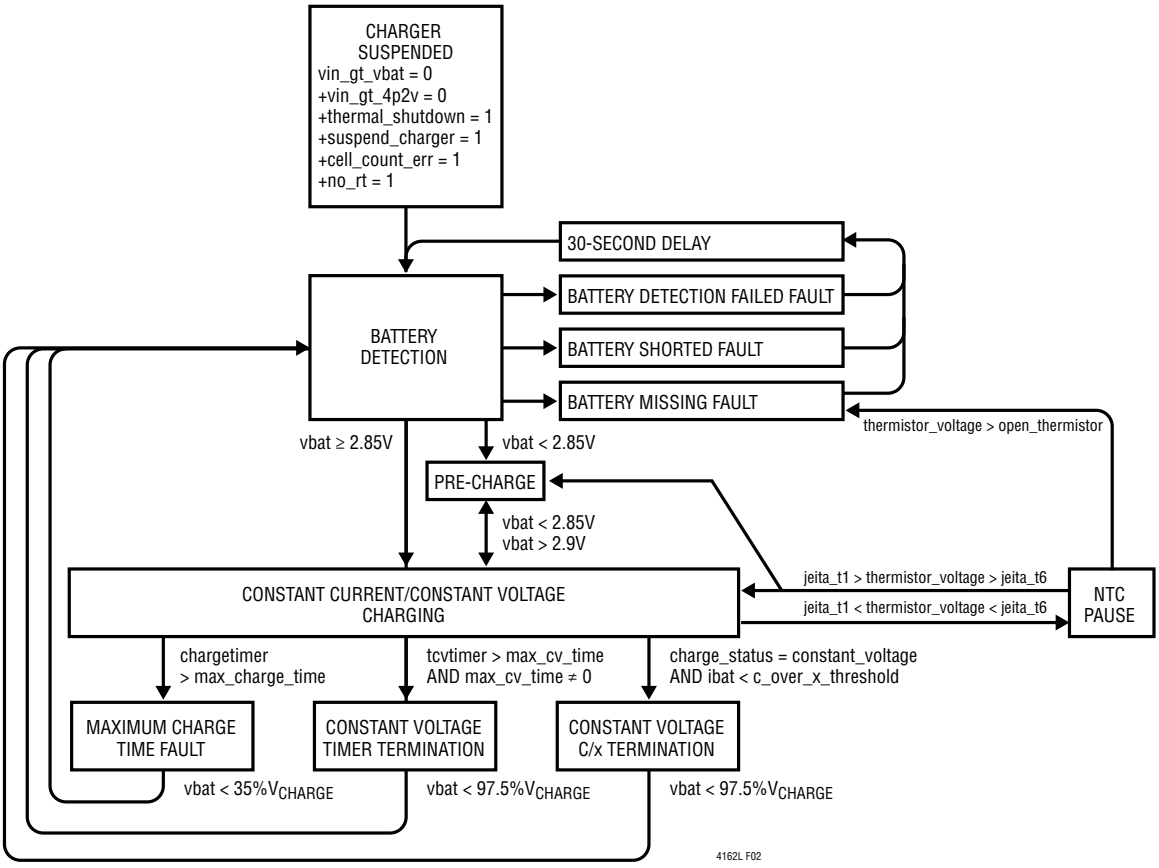


**Figure 2. Battery Charging State Diagram**

# OPERATION

### Low Power Ship Mode

The LTC4162 can reduce its already low battery-only standby current to about 2.8µA in a special mode designed for shipment and storage. Ship mode is armed by setting arm_ship_mode to arm. It does not take effect, however, until the input voltage $V_{IN}$ drops below approximately 1V. Upon return of the input voltage above approximately 1V the LTC4162 wakes from ship mode. The decision to remain out of ship mode is latched once the internal voltage reference is re-biased and $V_{IN}$ is detected as having reached about 4.2V (vin_gt_4p2v). In ship mode, the VCC2P5 2.5V logic LDO and the $INTV_{CC}$ 5V system LDO are deactivated and, along with them, all logic and communications with the $I^2C$ port. Consequently, no settings or state information will persist through a ship mode cycle.

### Oscillator Synchronization

The SYNC pin is available to synchronize the switching battery charger to an external clock for optimum noise immunity. To use the SYNC pin, use the $R_T$ pin to set the frequency of the internal oscillator to the frequency expected by the SYNC signal. If no signal is present at SYNC, the internal oscillator will run normally. If a signal within the required tolerance range appears at SYNC, the internal oscillator will detect it and synchronize with it. To avoid a long or short cycle, synchronization won't occur until the internal oscillator and external signals coincide. Therefore, synchronization may take several thousand cycles (milliseconds) to occur. If SYNC is not used, it should just be grounded.

### Under Voltage Lockout Circuits/suspend_charger/ System Faults

Various supply monitor circuits, as well as suspend_charger, can disable charging. If the voltage at $V_{IN}$ falls below BATSENS+ (i.e. not vin_gt_vbat), or thermal_shutdown (die temperature above ~150°C), no_rt resistor, not intvcc_gt_2p8v, not vin_gt_4p2v, or a CELLS0/1 pins cell_count_err, the LTC4162 suspends charging and reports charger_suspended. In the absence of any of the above fault conditions, charging is re-enabled when $V_{IN}$ rises $V_{IN_DUVLO}$ above the BATSENS+ voltage.

### LTC4162 Lithium-Ion/Polymer Variants

The LTC4162-LAD is fully programmable and follows the descriptions given thus far but there are three other non-programmable voltage variants available as well. Each of these four versions is available with and without solar panel Maximum Power Tracking enabled by default.

The LTC4162 Lithium-Ion/Polymer variants are:

LTC4162-L40

LTC4162-L41

LTC4162-L42

LTC4162-LAD

The LTC4162-L40, LTC4162-L41 and LTC4162-L42 JEITA values are not writable and follow the values outlined below.

| | jeita_t1 **0x3EF5 (0°C)** | jeita_t2 **0x3721 (10°C)** | jeita_t3 **0x1F22 (40°C)** | jeita_t4 **0x1BC8 (45°C)** | jeita_t5 **0x18B5 (50°C)** | jeita_t6 **0x136A (60°C)** | |
|---|---|---|---|---|---|---|---|
| **VARIANT** | **REGION1** | **REGION2** | **REGION3** | **REGION4** | **REGION5** | **REGION6** | **REGION7** |
| **CHARGE CURRENT** | CHARGER OFF | 16mV/$R_{SNSB}$ | 32mV/$R_{SNSB}$ | 32mV/$R_{SNSB}$ | 16mV/$R_{SNSB}$ | 16mV/$R_{SNSB}$ | CHARGER OFF |
| LTC4162-L40 | | 4.0V | 4.0V | 3.9V | 3.9V | 3.95V | |
| LTC4162-L41 | | 4.1V | 4.1V | 4.0V | 4.0V | 4.05V | |
| LTC4162-L42 | | 4.2V | 4.2V | 4.1V | 4.1V | 4.05V | |
| LTC4162-LAD | | 4.2V | 4.2V | 4.1V | 4.1V | 4.05V | |

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### SMBus and I²C Protocol Compatibility

The LTC4162 uses an SMBus/I²C style 2-wire serial port for some programming and all monitoring functions. Over the serial port the user may program alert values which are compared against measured parameters, set control parameters and read status data. The Timing Diagram shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors are required on these lines. The LTC4162 is both a slave receiver and slave transmitter. It is never a master. The control signals, SDA and SCL, are scaled internally to the $DV_{CC}$ supply for compliance with the I²C specification. $DV_{CC}$ should be connected to the same power supply as the bus pull-up resistors.

Aside from electrical levels and bus speed, the SMBus specification is generally compatible with the I²C specification, but extends beyond I²C to define and standardize specific formats for various types of transactions. The LTC4162 serial port is compatible with the 0Hz-400kHz speed and ratiometric input thresholds of the I²C specification, but supports both the Read-Word and Write-Word protocols of the SMBus specification, either with or without packet error checking (PEC). The SMBALERT and ARA protocols of the SMBus specification are also supported. Finally, it has built-in timing delays and glitch suppression filters to ensure correct operation with both protocols.

The input logic levels of I²C and SMBus are specified differently. I²C specifies logic levels that are ratiometric to supply and SMBus specifies absolute levels. By comparing the specifications, it can be shown that the logic levels are compatible for supply voltages ranging from 2.667V to 3.000V, however, with a well designed system, I²C compatible and SMBus compatible parts are often found to be interchangeable. Appendix B of System Management Bus (SMBus) Specification Version 2.0 highlights differences between SMBus and I²C, as does section 4 of I²C-bus Specification and User Manual.

### Alternate Thermistors and Biasing

Thermistors with a β value higher than 3490K may be used with the LTC4162 by either diluting the thermistor with an inexpensive low drift series resistor, $R_{SERIES}$, or overwriting jeita_t1 through jeita_t6 with appropriate values. If a single dilution resistor is added, $R_{NTCBIAS}$ should be increased by an amount equal to the dilution resistor to pad the bias resistor, thereby returning the resistor ratio to 50% and, therefore, yielding no error at 25°C. Slightly more padding of $R_{NTCBIAS}$ may be desired to lift and center the error curve over a given temperature range. With the addition of one more resistor, $R_{PARALLEL}$, to the thermistor bias network, it's possible to further refine the temperature profile of a higher β thermistor to match the expected β value of 3490K. The values of $R_{NTCBIAS}$, $R_{PARALLEL}$ and $R_{SERIES}$ can be selected to nearly match the thermistor profile expected by the LTC4162. An example is included here as a demonstration.

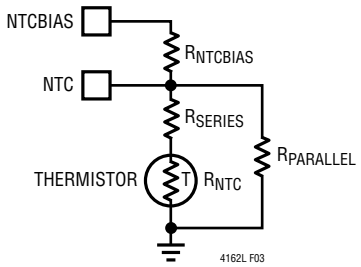


**Figure 3. Diluting the Thermistor with Low Drift Series and Parallel Resistors**

For a 10k Vishay NTCS0402E3103FHT thermistor which has a $\beta_{25/75}$ value of 3950K, using $R_{NTCBIAS}$ = 10k, $R_{SERIES}$ = 549 and $R_{PARALLEL}$ = 187k will closely mimic the profile of a thermistor β value of 3490K over the 0°C to 60°C range resulting in a nominal error of under ±0.5°C for the default JEITA temperature thresholds defined by jeita_t1 through jeita_t6. This error is significantly less than the error tolerance of most thermistors.

## APPLICATIONS INFORMATION

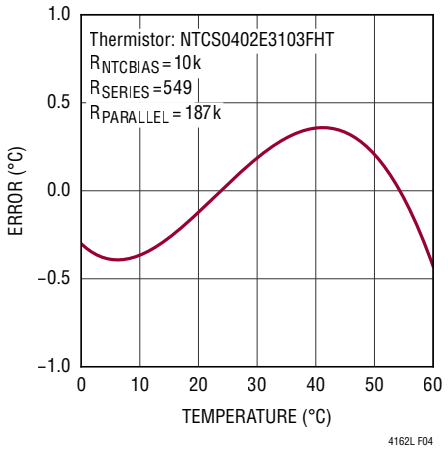


**Figure 4. Residual Error from 0°C to 60°C for a $\beta_{25/75}$ = 3950K Thermistor**

For tools that can assist with alternate thermistors, please visit the LTC4162 web page.

### Programming the Input and Battery Charge Current Limits

The LTC4162 features independent resistor programmability of the input current and battery charge current upper limits to facilitate optimal charging from a wide variety of input power sources. The battery charge current should be programmed solely on the basis of the size of the battery and its associated safe charging rate. Typically, this rate is about "1C", or equal to the current which would discharge the battery in one hour. For example, a 2000mAh battery would be charged with no more than 2A. With the full scale (default) charge current programmed via the resistor, $R_{SNSB}$, between CSP and CSN, all other selectable charge current settings are lower and may be appropriate for custom charge algorithms at extreme temperatures. If the battery charge current limit requires more power than is available from the selected input current limit, the input current limit will be enforced and the battery will be charged with less than the programmed current. Thus, the battery charger sense resistor should be programmed based on the battery capacity only, without concern for the input source.

The maximum average input current is determined by the sense resistor, $R_{SNSI}$, connected between the CLP and CLN pins. Its value should be chosen based only on the maximum available current limit of the expected input source. The input and charge current loops servo the voltages across their respective sense resistors to a maximum of 32mV, giving maximum input and charge currents of:

$$I_{IN(MAX)} = 32mV/R_{SNSI}$$

$$I_{CHG(MAX)} = 32mV/R_{SNSB}$$

The charge current and input current sense resistors convert the charge and input currents into a voltage measurable by the LTC4162. The accuracy and temperature coefficient of the current sense resistors contribute directly to the current regulation accuracy of the LTC4162. While 4-terminal resistors are available for current sensing applications, simpler 2-terminal resistors provide a more economical solution. Power dissipation of the sense resistors should be carefully considered. For example, with a 3.2A charge current the sense resistor would be 10mΩ and power dissipation would be $3.2^2A^2 \bullet 10m\Omega = 102.4mW$. While a 1/8W 0603 resistor is theoretically feasible in this application, its temperature rise could be quite high. A 1/4W to 1/2W 0805 resistor might be a better choice for lower thermal rise and subsequently better accuracy. Using larger copper pours and having more copper coverage will reduce the thermal resistance of the sense resistors. Figure 5 shows an example of a proper Kelvin connection to the current sense resistors.

**Figure 5. Kelvin Current Sensing with an 0805 Resistor.**

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### Power Path Isolation in Ship Mode

In ship mode, the LTC4162 shuts down nearly all internal circuits and reduces its quiescent current to only a few micro-Amperes. The body diodes of the power path transistors still provide a conduction path from the battery to the system load however. If circuits down stream of the LTC4162 power path must be completely cut off in ship mode, an external PMOS transistor and one small signal NMOS transistor can provide this isolation. The circuit of Figure 6 exploits the fact that the VCC2P5 pin drops to ground in ship mode. MP1 should be chosen to have a fairly low threshold voltage if full conductance is needed for single cell applications because in the single cell case MN1 drops out and $R_A$ and $R_B$ form a voltage divider preventing full gate drive to MP1.

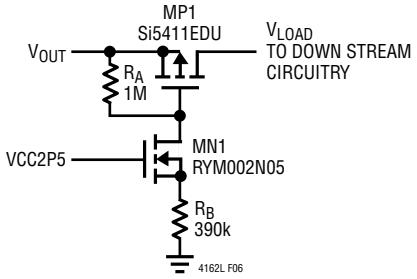


**Figure 6. Isolating Downstream Circuits in Ship Mode.**

### Choosing the BOOST Capacitor

The BOOST capacitor should be a low ESR surface mount ceramic type rated to at least 6.3V and should have a value of 22nF.

### Choosing the Inductor

To ensure proper ripple current and control loop stability the inductor value as a function of switching frequency and maximum input voltage should be computed from the following expression:

$$L(\mu H) = \frac{0.3 \bullet V_{IN(MAX)}}{f_{OSC}(MHz)}$$

Once the value for L is known, the type of inductor core must be selected. Ferrite cores are recommended for their very low core loss at frequencies above 100kHz, such as is the operating frequency of the LTC4162. Ferrite core material saturates hard, however, which means that inductance collapses abruptly when the peak design current is exceeded. This causes an abrupt increase in inductor ripple current and consequent output voltage ripple. The saturation current for the inductor should be about 30% higher than the maximum regulated current, $I_{CHG(MAX)}$.

### Setting the Switching Frequency ($R_T$ Resistor)

The operating frequency and inductor selection are interrelated. Higher operating frequencies allow the use of smaller inductors and capacitors but generally also results in lower efficiency because of switching and charge transfer losses. The feedback loops of LTC4162 are internally compensated and cannot be adjusted. The LTC4162 is designed to operate properly with frequencies ranging from 1MHz to 2.5MHz. Operation at lower or higher frequencies jeopardizes control loop stability. A resistor on the $R_T$ pin sets the LTC4162's step-down switching charger operating frequency. To keep the inductor size down and ensure peak efficiency and stability, the LTC4162 has been optimized to run at 1.5MHz with an $R_T$ value of 63.4kΩ. Small changes in oscillator frequency can be achieved by altering $R_T$ from this value. The oscillator frequency is inversely proportional to $R_T$ as given by the expression:

$$f_{OSC}(MHz) = \frac{94}{R_T(k\Omega)}$$

### Choosing the $V_{OUT}$, BATSENS+, $INTV_{CC}$ and VCC2P5 Bypass Capacitors

The style and value of the capacitors used with the LTC4162 determine important parameters, such as regulator control loop stability and input voltage ripple. Because the LTC4162 uses a step-down switching power supply from $V_{OUT}$ to BATSENS+, its input current waveform contains very high frequency components. It is imperative that low equivalent

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series resistance (ESR) multilayer ceramic capacitors be used to bypass $V_{OUT}$. Tantalum and aluminum capacitors will not work because of their high ESR and ESL. The value of the total capacitance on $V_{OUT}$ directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple. The LTC4162 has been designed with $V_{OUT}$ and PGND as two corner pin groups so there is ample room to fit an appropriate bypass capacitor. The need for low impedance capacitance directly adjacent to the $V_{OUT}$ and PGND pins cannot be overemphasized. PCB distance of only a few millimeters will introduce nano-Henrys of inductance and compromise the high frequency "hot-loop" (See Printed Circuit Board Layout Considerations).

It is also recommended that a ceramic capacitor be used to bypass BATSENS+. At least 10µF with low ESR is required. Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

The $INTV_{CC}$ and VCC2P5 pins are the outputs of onboard low dropout regulators and also require ceramic capacitors. The $INTV_{CC}$ and VCC2P5 capacitors should be as close to the LTC4162 as possible and returned immediately to an analog ground plane. The $INTV_{CC}$ pin requires at least 4.7µF of capacitance rated to at least 6.3V and the VCC2P5 pin requires at least 1µF rated to 4V.

The actual capacitance of any ceramic capacitor should be measured with a small AC signal and DC bias, as is expected in-circuit. Many vendors specify the capacitance versus voltage with a $1V_{RMS}$ AC test signal with no bias and, as a result, grossly overstate the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure, or request from the vendor, the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

### INFET and BATFET MOSFET Selection

An external N-channel MOSFET is required for both the input and battery paths. Important parameters for the selection of these MOSFETs are the maximum drain-source voltage, $V_{DSS}$, gate threshold voltage and on-resistance ($R_{DS(ON)}$). When the input is grounded, the battery stack voltage is applied across the input MOSFET. When $V_{BAT}$ is at 0V, the input voltage is applied across the battery MOSFET. Therefore, the $V_{DSS}$ of the input MOSFET must withstand the maximum voltage on $V_{BAT}$ while the $V_{DSS}$ of the output MOSFET must withstand the highest voltage on $V_{IN}$. The gate drive for both is 5V. This requires the use of logic-level threshold N-channel MOSFETs. As a general rule, select MOSFETs with a low enough $R_{DS(ON)}$ to obtain the desired $V_{DS}$ and power dissipation while operating at full load current.

### Operation Without a Battery

The LTC4162 has built in battery detection. Its switching regulator will generally not start if the battery is missing. However, if a battery is present at the beginning of a charge cycle and is removed, the LTC4162 will operate without a battery. Typically the BATSENS+ pin will rise quickly to the programmed constant-voltage level and remain there. However, it is important that the impedance on the BATSENS+ node be kept relatively low at the switching frequency. Therefore a ceramic capacitor of 10µF or more near the LTC4162 is necessary. Note that without a load on the BATSENS+ pin, the switching regulator will eventually terminate due to tcvtimer reaching max_cv_time.

### Operation With Long Battery Leads

The LTC4162 is generally resilient to operation with long battery leads, however a ceramic capacitor of 10µF or more of appropriate voltage tolerance near the LTC4162 is necessary. Note that any parasitic battery resistance, such as long cabling, will push the LTC4162 into constant voltage charging sooner, dramatically extending charging

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time. If possible, the BATSENS+ pin should be connected to the battery terminals with a separate Kelvin connection from that of the current carrying inductor path. The bulk load capacitor should be on the inductor side of this connection, not the BATSENS+ side. A smaller ceramic capacitor may additionally be added to the BATSENS+ pin near the LTC4162. A heavy copper run from the low side of battery to the GND (paddle) of the LTC4162 is also necessary to reduce resistance optimizing charging time.

### Resistive Inputs and Test Equipment

Care must be exercised in the laboratory while evaluating the LTC4162 with inline ammeters. The combined resistance of the internal current sense resistor and fuse of many meters can be 0.5Ω or more. At currents of 3A+ it is possible to drop several volts across the meter and wiring, possibly resulting in unusual voltage readings or artificially high switch duty cycles. A resistive connection to the source of input power can be particularly troublesome. With the undervoltage limit feature enabled, the switching regulator output power will be automatically reduced to prevent $V_{IN}$ from falling below its programmed level. This feature greatly improves tolerance to resistive input power sources (from either undersized wiring and connectors or test equipment) and facilitates stable behavior, but if engaged, could result in much less power delivery to the battery.

### Solar Panel Input Impedance Correction

The maximum power point tracking algorithm uses the LTC4162's input voltage regulation control loop to find and operate at the maximum power point of the solar panel. In general solar panels have two distinct regions of operation roughly corresponding to constant voltage and constant current. In its constant voltage region the panel presents a somewhat low impedance and in its constant current region a very high impedance. Figure 7 shows an I-V characteristic collected from a brightly lit high quality 40W solar panel. Notice the very high impedance below 16V and fairly low impedance above 16V.

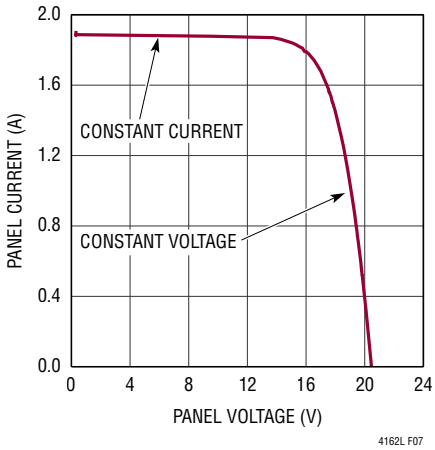


**Figure 7. High Quality 40W Solar Panel**

When the driving impedance is at or below a few Ohms the LTC4162's input voltage regulation loop is very stable. However, in its attempt to find the maximum power point, the LTC4162 drags the panel voltage down to its constant-current high impedance region. In this region the LTC4162 input voltage control loop will become unstable. To avoid instability and UVLO restarts the real input impedance of the LTC4162 should be maintained at about 2.5Ω in the 1kHz to 10kHz band. To achieve this characteristic an R-C network should be added to the solar panel. For example, a lower quality 100µF to 1000µF capacitor plus a 2.5Ω series resistor would make a good impedance correction network as shown in Figure 8.

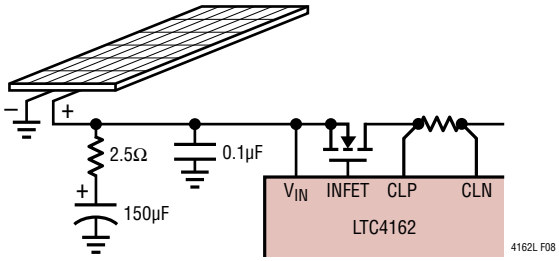


**Figure 8. Input Impedance Compensation Network**

Figure 9 shows the driving impedance presented by the combined solar panel plus 10µF bypass capacitor on $V_{OUT}$ in both low impedance and high impedance solar panel regions. In the low impedance region the aggregate impedance characteristic is about one to three Ohms in parallel

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with a 10µF capacitor. Also shown is the troublesome constant-current region where the impedance is essentially that of just the 10µF bypass capacitor. Two other networks are shown comprising a larger 100µF and 1000µF capacitor both in series with a 2.5Ω resistor for impedance flattening and phase shift mitigation. The compensation capacitor should be a solid or "polymer" electrolytic type such as the Panasonic ZA hybrid series to preserve stable ESR over temperature. Conventional, or "wet", electrolytic capacitors should be avoided as their ESR increases dramatically at low temperature. The larger compensation capacitor will create a wider impedance flattening frequency range and therefore more stable operation.

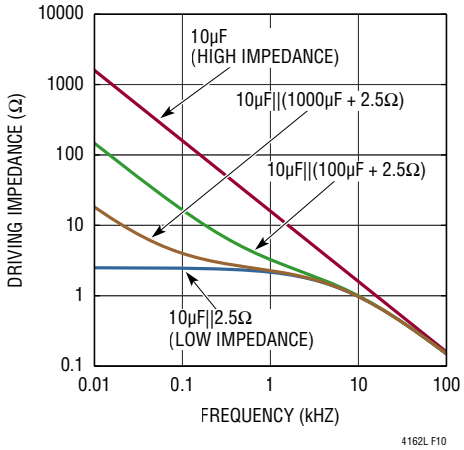


**Figure 9. Aggregate Input Impedance vs Frequency**

### USB Power Delivery

For 1 to 4 cell Lithium-Ion products, the LTC4162 can support the USB Power Delivery specification. Table 7 shows the relevant compatibility of cell_count vs USB profile.

**Table 7. Cell Count Support vs USB Power Delivery Profile**

| USB PD Voltage | 1 Cell Product | 2 Cell Product | 3 Cell Product | 4 Cell Product |
|---|---|---|---|---|
| 5V | ✔ | ✘ | ✘ | ✘ |
| 9V | ✔ | ✔ | ✘ | ✘ |
| 15V | ✔ | ✔ | ✔ | ✘ |
| 20V | ✔ | ✔ | ✔ | ✔ |

### Battery and Input Voltage Hot Plugging

Aluminum-polymer, aluminum-electrolytic or tantalum capacitors can minimize overshoot when hot plugging a battery or power connector. Ceramic capacitors are required close to the LTC4162 $V_{OUT}$ pins to supply very high frequency switching current but their extreme nonlinearity produces excessively high overshoot during hot plug. Their capacitance typically plunges by more than 80% as the voltage increases from 0V to rated voltage. This nonlinearity encourages high current at low voltage while rapidly shedding capacitance as the voltage rises; a dangerous combination resulting in high voltage overshoot. Empirically, the combination of a ceramic capacitor near the LTC4162 and a lower Q, voltage-stable, aluminum type capacitor provides the most robust combination. TVS diodes may also be used to limit voltage overshoot on either the input connector or the battery connector of a portable product. A single protection device (lossy capacitor or TVS) on the $V_{OUT}$ terminal may be sufficient to handle hot plug events from either the battery or the input connector as the power path MOSFETs diode-OR to the $V_{OUT}$ node. For solar panel applications the solar panel compensation network may provide adequate hot plug protection on the input terminal. See Application Note AN88 for examples.

### Printed Circuit Board Layout Considerations

The Exposed Pad on the backside of the LTC4162 must be securely soldered to the PC board ground. It serves as the analog ground pin and thermal sink. There should be a group of vias under the grounded backside leading directly down to an internal unbroken ground plane.

High frequency currents tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural, least-area, path, excessive voltage will build up and radiated emissions will occur (see Figure 10). To

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minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (i.e. layer 2).

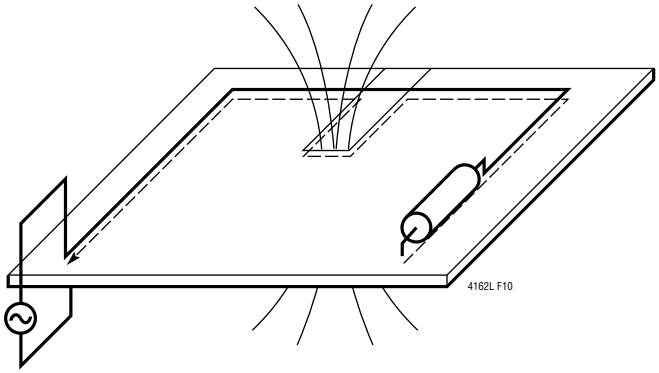



**Figure 10. Currents Tend to Follow Their Natural Least Area Path. Breaks in the Ground Plane Lead to Increased Impedance and EMI**

The capacitor from $V_{OUT}$ to PGND is the most critical high frequency component. It's proximity to the LTC4162 should be prioritized above all else. The LTC4162 is designed to have this capacitor placed directly adjacent to the short side of the package where the connections to pins (27,28) and (23,24) can be made on the top copper layer of the PC board (see Figures 12 and 13). The inductor connection to SW should feed out between the input capacitor terminals or down to a lower layer with a group of vias very close to the LTC4162.

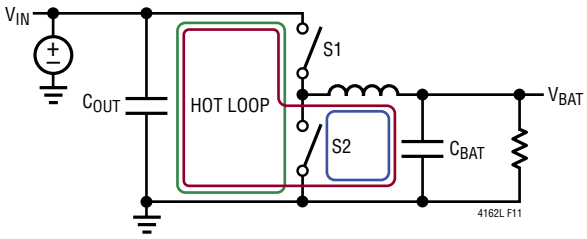



**Figure 11. Hot Loop**

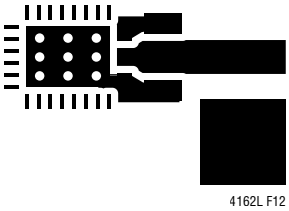



**Figure 12. Recommended Placement of the $V_{OUT}$ Bypass Capacitor and Inductor**

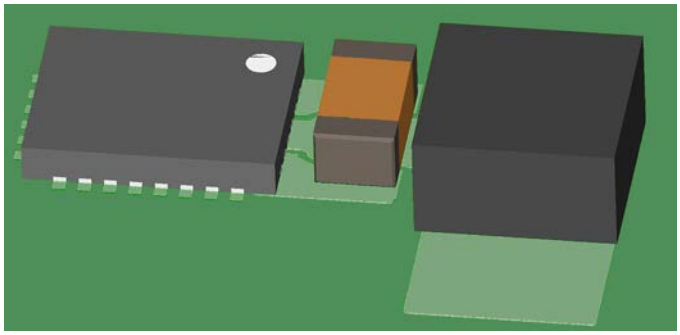


**Figure 13. Recommended Placement of the $V_{OUT}$ Bypass Capacitor and Inductor**

Due to its high frequency switching circuitry, it is also imperative that the $INTV_{CC}$ and VCC2P5 LDO capacitors as well as the BOOST-SW capacitor be as close to the LTC4162 as possible. Additionally, minimizing the SW pin trace area will help minimize high frequency radiated energy.

The ceramic capacitor on BATSENS+ carries the inductor ripple current. While not as critical as the $V_{OUT}$ bypass capacitor, an unbroken copper pour from this capacitor's low side to the LTC4162 PGND pins (23, 24) and the analog ground pin (paddle) will reduce output voltage ripple and ensure proper regulation.

The LTC4162 demonstration board DC2038A provides an excellent example of a suitable PC board layout.

# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| **vbat_lo_alert_limit** | 0x01 | R/W | [15:0] | 0 | Signed number that sets a lower limit that can be used to trigger an interrupt based on the per-cell battery voltage out of range. The value is based on the A/D value, vbat, which has a scaling factor of cell_count × 192.4µV/LSB. To compute the per-cell bit count, divide the desired trigger voltage by both cell_count and 192.4µV. The alert is enabled by setting en_vbat_lo_alert and can be read back and cleared at vbat_lo_alert. |
| **vbat_hi_alert_limit** | 0x02 | R/W | [15:0] | 0 | Signed number that sets an upper limit that can be used to trigger an interrupt based on the per-cell battery voltage out of range. The value is based on the A/D value, vbat, which has a scaling factor of cell_count × 192.4µV/LSB. To compute the per-cell bit count, divide the desired trigger voltage by both cell_count and 192.4µV. The alert is enabled by setting en_vbat_hi_alert and can be read back and cleared at vbat_hi_alert. |
| **vin_lo_alert_limit** | 0x03 | R/W | [15:0] | 0 | Signed number that sets a lower limit that can be used to trigger an interrupt based on input voltage out of range. The value is based on the A/D value, vin, which has a scaling factor of 1.649mV/LSB. The alert is enabled by setting en_vin_lo_alert and can be read back and cleared at vin_lo_alert. |
| **vin_hi_alert_limit** | 0x04 | R/W | [15:0] | 0 | Signed number that sets an upper limit that can be used to trigger an interrupt based on input voltage out of range. The value is based on the A/D value, vin, which has a scaling factor of 1.649mV/LSB. The alert is enabled by setting en_vin_hi_alert and can be read back and cleared at vin_hi_alert. |
| **vout_lo_alert_limit** | 0x05 | R/W | [15:0] | 0 | Signed number that sets a lower limit that can be used to trigger an interrupt based on vout voltage out of range. The value is based on the A/D value, vout, which has a scaling factor of 1.653mV/LSB. The alert is enabled by setting en_vout_lo_alert and can be read back and cleared at vout_lo_alert. |
| **vout_hi_alert_limit** | 0x06 | R/W | [15:0] | 0 | Signed number that sets an upper limit that can be used to trigger an interrupt based on vout voltage out of range. The value is based on the A/D value, vout, which has a scaling factor of 1.653mV/LSB. The alert is enabled by setting en_vout_hi_alert and can be read back and cleared at vout_hi_alert. |
| **iin_hi_alert_limit** | 0x07 | R/W | [15:0] | 0 | Signed number that sets an upper limit that can be used to trigger an interrupt based on input current out of range. The value is based on the A/D value, iin, which has a scaling factor of 1.466µV / RSNSI amperes/LSB. The alert is enabled by setting en_iin_hi_alert and can be read back and cleared at iin_hi_alert. |
| **ibat_lo_alert_limit** | 0x08 | R/W | [15:0] | 0 | Signed number that sets a lower limit that can be used to trigger an interrupt based on charge current dropping below a particular value, such as during the constant-voltage phase of charging, or, load current exceeding a particular limit when not charging. When the charger is not running, and telemetry is enabled with force_telemetry_on, this limit indicates that the battery draw has exceeded a particular value. Telemetry will be enabled automatically if the input voltage exceeds the battery voltage, in which case discharge current will be nearly zero. ibat values are positive for charging and negative for discharging so the polarity of this register should be set according to the mode in which the limit alert is of interest. The value is based on the A/D value, ibat, which has a scaling factor of 1.466µV / RSNSB amperes/LSB. The alert is enabled by setting en_ibat_lo_alert and can be read back and cleared at ibat_lo_alert. |
| **die_temp_hi_alert_limit** | 0x09 | R/W | [15:0] | 0 | Signed number that sets an upper limit that can be used to trigger an interrupt based on high die temperature. The value in °C can be calculated from the A/D reading, die_temp, as TDIE(°C) = die_temp × 0.0215°C/LSB - 264.4°C. The alert is enabled by setting en_die_temp_hi_alert and can be read back and cleared at die_temp_hi_alert. |
| **bsr_hi_alert_limit** | 0x0A | R/W | [15:0] | 0 | Sets an upper limit that can be used to trigger an interrupt based on high battery resistance. The per-cell battery resistance is relative to the battery charge current setting resistor, RSNSB, and can be computed in Ω from: BSR = cell_count × bsr × RSNSB / 500. The alert is enabled by setting en_bsr_hi_alert and can be read back and cleared at bsr_hi_alert. |

# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| **thermistor_voltage_hi_alert_limit** | 0x0B | R/W | [15:0] | 0 | Signed number that sets an upper limit that can be used to trigger an interrupt based on thermistor value out of range. The value is based on the A/D value for thermistor_voltage. The thermistor value can be determined by the expression RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so higher temperatures correspond to lower thermistor_voltage readings and vice-versa. The alert is enabled by setting en_thermistor_voltage_hi_alert can be read back and cleared at thermistor_voltage_hi_alert. |
| **thermistor_voltage_lo_alert_limit** | 0x0C | R/W | [15:0] | 0 | Signed number that sets a lower limit that can be used to trigger an interrupt based on thermistor value out of range. The value is based on the A/D value for thermistor_voltage. The thermistor value can be determined by the expression RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so higher temperatures correspond to lower thermistor_voltage readings and vice-versa. The alert is enabled by setting en_thermistor_voltage_lo_alert and can be read back and cleared at thermistor_voltage_lo_alert. |
| **EN_LIMIT_ALERTS_REG** | 0x0D | R/W | [15:0] | 0 | Enable limit monitoring and alert notification via SMBALERT |
| en_telemetry_valid_alert | | | [15] | 0 | To ensure high measurement accuracy, the telemetry system in the LTC4162 has a nominal start-up time of approximately 12ms. Setting this interrupt request causes an SMBALERT telemetry_valid_alert when telemetry_valid indicates that the telemetry system's readings are valid. Note that the switching battery charger will not operate until this telemetry system warmup period has passed, regardless of the state of this setting. |
| en_bsr_done_alert | | | [14] | 0 | Interrupt request that causes an SMBALERT upon bsr_done_alert when the bsr (battery-series-resistance) measurement is finished. |
| en_vbat_lo_alert | | | [11] | 0 | Interrupt request that causes an SMBALERT upon vbat_lo_alert when vbat is below vbat_lo_alert_limit. |
| en_vbat_hi_alert | | | [10] | 0 | Interrupt request that causes an SMBALERT upon vbat_hi_alert when vbat is above vbat_hi_alert_limit. |
| en_vin_lo_alert | | | [9] | 0 | Interrupt request that causes an SMBALERT upon vin_lo_alert when vin is below vin_lo_alert_limit. |
| en_vin_hi_alert | | | [8] | 0 | Interrupt request that causes an SMBALERT upon vin_hi_alert when vin is above vin_hi_alert_limit. |
| en_vout_lo_alert | | | [7] | 0 | Interrupt request that causes an SMBALERT upon vout_lo_alert when vout is below vout_lo_alert_limit. |
| en_vout_hi_alert | | | [6] | 0 | Interrupt request that causes an SMBALERT upon vout_hi_alert when vout is above vout_hi_alert_limit. |
| en_iin_hi_alert | | | [5] | 0 | Interrupt request that causes an SMBALERT upon iin_hi_alert when iin is above iin_hi_alert_limit. |
| en_ibat_lo_alert | | | [4] | 0 | Interrupt request that causes an SMBALERT upon ibat_lo_alert when ibat is below ibat_lo_alert_limit. |
| en_die_temp_hi_alert | | | [3] | 0 | Interrupt request that causes an SMBALERT upon die_temp_hi_alert when die_temp is above die_temp_hi_alert_limit. |
| en_bsr_hi_alert | | | [2] | 0 | Interrupt request that causes an SMBALERT upon bsr_hi_alert when bsr is above bsr_hi_alert_limit. |
| en_thermistor_voltage_hi_alert | | | [1] | 0 | Interrupt request that causes an SMBALERT upon thermistor_voltage_hi_alert when thermistor_voltage is above thermistor_voltage_hi_alert_limit. Recall that the thermistor has a negative temperature coefficient so higher thermistor_voltage readings correspond to lower temperatures. |
| en_thermistor_voltage_lo_alert | | | [0] | 0 | Interrupt request that causes an SMBALERT upon thermistor_voltage_lo_alert when thermistor_voltage is below thermistor_voltage_lo_alert_limit. Recall that the thermistor has a negative temperature coefficient so lower thermistor_voltage readings correspond to higher temperatures. |

## REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| **EN_CHARGER_STATE_ALERTS_REG** | 0x0E | R/W | [12:0] | 0 | Enable charger state notification via SMBALERT |
| en_bat_detect_failed_fault_alert | | | [12] | 0 | Interrupt request that causes an SMBALERT upon bat_detect_failed_fault_alert as indicated by bat_detect_failed_fault due to an inability to source power to the battery during battery detection testing (usually due to either iin_limit_active or vin_uvcl_active). |
| en_battery_detection_alert | | | [11] | 0 | Interrupt request that causes an SMBALERT upon battery_detection_alert as indicated by battery_detection due to the LTC4162 entering battery detection testing. |
| en_charger_suspended_alert | | | [8] | 0 | Interrupt request that causes an SMBALERT upon charger_suspended_alert as indicated by charger_suspended whereby battery charging is terminated due to suspend_charger or thermistor_voltage out of jeita_t1 - jeita_t6 range. |
| en_precharge_alert | | | [7] | 0 | Interrupt request that causes an SMBALERT upon precharge_alert as indicated by precharge denoting the onset of the precharge phase of a battery charging cycle. |
| en_cc_cv_charge_alert | | | [6] | 0 | Interrupt request that causes an SMBALERT upon cc_cv_charge_alert as indicated by cc_cv_charge denoting the onset of the constant current / constant voltage phase of a battery charging cycle. |
| en_ntc_pause_alert | | | [5] | 0 | Interrupt request that causes an SMBALERT upon ntc_pause_alert as indicated by ntc_pause whereby a battery charge cycle is interrupted due to thermistor_voltage out of range as set by the jeita_t1 through jeita_t6 values. |
| en_timer_term_alert | | | [4] | 0 | Interrupt request that causes an SMBALERT upon timer_term_alert as indicated by timer_term whereby a battery charge cycle terminates due to tcvtimer reaching max_cv_time, the maximum time allowed in constant_voltage mode. |
| en_c_over_x_term_alert | | | [3] | 0 | Interrupt request that causes an SMBALERT upon c_over_x_term_alert as indicated by c_over_x_term whereby a battery charge cycle terminates due to ibat dropping below the c_over_x_threshold. |
| en_max_charge_time_alert | | | [2] | 0 | Interrupt request that causes an SMBALERT upon max_charge_time_fault_alert as indicated by max_charge_time_fault whereby charging has terminated due to tchargetimer reaching max_charge_time. |
| en_bat_missing_fault_alert | | | [1] | 0 | Interrupt request that causes an SMBALERT upon bat_missing_fault_alert as indicated by bat_missing_fault whereby charging is prohibited if no battery is detected during the battery presence detection phase at the beginning of a charge cycle. |
| en_bat_short_fault_alert | | | [0] | 0 | Interrupt request that causes an SMBALERT upon bat_short_fault_alert as indicated by bat_short_fault whereby charging is prohibited if a shorted battery is detected during the battery presence detection phase at the beginning of a charge cycle. |
| **EN_CHARGE_STATUS_ALERTS_REG** | 0x0F | R/W | [5:0] | 0 | Enable charge status notification via SMBALERT |
| en_ilim_reg_active_alert | | | [5] | 0 | Interrupt request that causes an ilim_reg_active_alert SMBALERT upon ilim_reg_active (VCSP-VCSN greater than 45mV). May indicates that the switching regulator is currently controlling power delivery based on a safety current limit. This should not occur under normal conditions and is likely the result of a circuit board fault. Alternately indicates that the switching regulator is in dropout (near 100% duty cycle) and is not regulating on any feedback control loop. |
| en_thermal_reg_active_alert | | | [4] | 0 | Interrupt request that causes a thermal_reg_active_alert SMBALERT upon thermal_reg_active indicating that the icharge_dac is being dialed back to reduce internal die heating. |
| en_vin_uvcl_active_alert | | | [3] | 0 | Interrupt request that causes a vin_uvcl_active_alert SMBALERT upon vin_uvcl_active indicating that the undervoltage regulation loop has taken control of the switching regulator. |
| en_iin_limit_active_alert | | | [2] | 0 | Interrupt request that causes a iin_limit_active_alert SMBALERT upon iin_limit_active indicating that the input current regulation loop has taken control of the switching regulator. |

# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| en_constant_ current_alert | | | [1] | 0 | Interrupt request that causes a constant_current_alert SMBALERT upon constant_current indicating that the battery charger constant current regulation loop has taken control of the switching regulator. |
| en_constant_ voltage_alert | | | [0] | 0 | Interrupt request that causes a constant_voltage_alert SMBALERT upon constant_voltage indicating that the battery charger constant voltage regulation loop has taken control of the switching regulator. |
| **thermal_reg_start_ temp** | 0x10 | R/W | [15:0] | 17897 | Signed number that sets the start of the temperature region for thermal regulation. To prevent overheating, a thermal regulation feedback loop utilizing die_temp sets an upper limit on icharge_dac following a linear gradient from full scale (31) to minimum scale (0) between thermal_reg_start_temp and thermal_reg_end_temp. The default value of 17897 corresponds to 120°C. |
| **thermal_reg_end_ temp** | 0x11 | R/W | [15:0] | 18130 | Signed number that sets the end of the temperature region for thermal regulation. To prevent overheating, a thermal regulation feedback loop utilizing die_temp sets an upper limit on icharge_dac following a linear gradient from full scale (31) to minimum scale (0) between thermal_reg_start_temp and thermal_reg_end_temp. The default value of 18130 corresponds to 125°C. |
| **CONFIG_BITS_REG** | 0x14 | R/W | [5:1] | 0 | System configuration settings |
| suspend_charger | | | [5] | 0 | Causes battery charging to be suspended. This setting should be used cautiously. For embedded battery systems where two wire interface communication relies on a minimum battery voltage, setting this bit could result in a deadlock that may require factory service to correct. |
| run_bsr | | | [4] | 0 | Causes the battery equivalent-series-resistance (bsr) measurement to be made as soon as a charge cycle starts or immediately if a charge cycle is already running. |
| telemetry_speed | | | [3] | 0 | Forces the telemetry system to take measurements at the higher rate of approximately once every 11ms whenever the telemetry system is on. When this bit is disabled, the telemetry system will slow down to about once every 5s to reduce power when not charging. Setting telemetry_speed to tel_high_speed in conjunction with force_telemetry_on with no input power available will increase battery drain.<br>Enums: tel_high_speed = 1,<br>tel_low_speed = 0 |
| force_telemetry_on | | | [2] | 0 | Causes the telemetry system to operate at all times, including times when only battery power is available. |
| mppt_en | | | [1] | 0 | Causes the Maximum Power-Point Tracking algorithm to run. The maximum power point algorithm takes control of the input undervoltage regulation control loop via the input_undervoltage_dac to seek the optimum power-point for resistive sources such as a long cable or solar panel. |
| **iin_limit_target** | 0x15 | R/W | [5:0] | 63 | Controls the target input current limit setting. The input current is limited by regulating charge current in response to the voltage across an external current sense resistor, RSNSI, between the CLP and CLN pins and is given by (iin_limit_target + 1) × 500µV / RSNSI. Note that the LTC4162 can only limit charge current based on this setting. It does not have the authority to block current from passing directly through to the system load. Connecting the system load to the battery, however, can allow total input current control. |
| **input_undervoltage_ setting** | 0x16 | R/W | [7:0] | 31 | Controls the input undervoltage regulation setting. The regulation voltage, given by (input_undervoltage_setting + 1) × 140.625mV, is the voltage at which the charge current will be reduced to prevent further droop in supply voltage due to a resistive source. If mppt_en is set, the MPPT algorithm will override this setting. The actual input undervoltage value can be read back from the input_undervoltage_dac. |
| **arm_ship_mode** | 0x19 | R/W | [15:0] | 0 | Setting this register to arm arms the ultra low-power ship and store mode. Ship mode does not take effect until the VIN pin drops below approximately 1V or immediately if VIN is already below 1V.<br>Enum: arm = 21325 |

## REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| **charge_current_setting** | 0x1A | R/W | [4:0] | 31 | Controls the target charge current regulation servo level. The charge current is regulated by servoing the voltage across an external current sense resistor, RSNSB, between the CSP and CSN pins. The servo voltage is given by (charge_current_setting + 1) × 1mV. The effective charge current, determined by the external resistor, RSNSB, is given by (charge_current_setting + 1) × 1mV / RSNSB. icharge_dac will follow charge_current_setting unless thermal_reg_active is true or the JEITA algorithm, with en_jeita, has altered it. |
| **vcharge_setting** | 0x1B | R/W | [4:0] | 31 | Controls the final charge voltage regulation servo level. To maintain inherent over-charge protection, only Lithium Ion appropriate charge voltage values can be selected. The charge voltage setting can be computed from cell_count × (vcharge_setting × 12.5mV + 3.8125V) where vcharge_setting ranges from 0 to 31 (4.2V max). vcharge_dac will follow vcharge_setting unless the advanced JEITA temperature control system (en_jeita) has altered it.<br>Enum: vcharge_lion_default = 31 |
| **c_over_x_threshold** | 0x1C | R/W | [15:0] | 2184 | Signed number that sets the ibat A/D value used to qualify C/x detection and termination. The C/x level is based on the value for ibat which has a scaling factor of 1.466µV / RSNSB amperes/LSB. For example, to make the C/x level C/10 (a very common choice) then c_over_x_threshold should be set to c_over_10 which is 10% of the maximum possible ibat reading (32mV × 37.5 × 18,191 / 10). 32mV is the full scale charge current signal from CSP to CSN, 37.5 is the internal charge amplifier's gain and 18,191 is the A/D's span term in counts per Volt.<br>Enum: c_over_10 = 2184 |
| **max_cv_time** | 0x1D | R/W | [15:0] | 14400 | Sets the constant-voltage termination setting against which the tcvtimer is compared. The timer begins at the onset of the constant_voltage phase of charging and increments at one count per second. The default setting is 14,400 (4 hours).<br>Enums: 30mins = 1800,<br>1hour = 3600,<br>2hours = 7200,<br>4hours_default = 14400 |
| **max_charge_time** | 0x1E | R/W | [15:0] | 0 | Sets the total charge time termination setting against which the tchargetimer is compared. The default value of 0 disables the total charge time feature and prevents the tchargetimer from running. If enabled with a non zero value, the tchargetimer begins counting at the onset of a charge cycle and increments at one count per minute.<br>Enum: maxchargetime_disable = 0 |
| **jeita_t1** | 0x1F | R/W | [15:0] | 16117 | Signed number that sets the JEITA temperature region transition temperature T1 between JEITA regions R1 and R2. The temperature is based on the thermistor reading from the telemetry system; RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so jeita_t1, representing colder temperatures, will have the highest value and jeita_t6, representing warmer temperatures, will have the lowest value. The default value of 16117 maps to about 0°C for the expected thermistor β value of 3490K. |
| **jeita_t2** | 0x20 | R/W | [15:0] | 14113 | Signed number that sets the JEITA temperature region transition temperature T2 between JEITA regions R2 and R3. The temperature is based on the thermistor reading from the telemetry system; RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so jeita_t1, representing colder temperatures, will have the highest value and jeita_t6, representing warmer temperatures, will have the lowest value. The default value of 14113 maps to about 10°C for the expected thermistor β value of 3490K. |
| **jeita_t3** | 0x21 | R/W | [15:0] | 7970 | Signed number that sets the JEITA temperature region transition temperature T3 between JEITA regions R3 and R4. The temperature is based on the thermistor reading from the telemetry system; RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so jeita_t1, representing colder temperatures, will have the highest value and jeita_t6, representing warmer temperatures, will have the lowest value. The default value of 7970 maps to about 40°C for the expected thermistor β value of 3490K. |

# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| **jeita_t4** | 0x22 | R/W | [15:0] | 7112 | Signed number that sets the JEITA temperature region transition temperature T4 between JEITA regions R3 and R4. The temperature is based on the thermistor reading from the telemetry system; RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so jeita_t1, representing colder temperatures, will have the highest value and jeita_t6, representing warmer temperatures, will have the lowest value. The default value of 7112 maps to about 45°C for the expected thermistor β value of 3490K. |
| **jeita_t5** | 0x23 | R/W | [15:0] | 6325 | Signed number that sets the JEITA temperature region transition temperature T5 between JEITA regions R5 and R6. The temperature is based on the thermistor reading from the telemetry system; RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so jeita_t1, representing colder temperatures, will have the highest value and jeita_t6, representing warmer temperatures, will have the lowest value. The default value of 6325 maps to about 50°C for the expected thermistor β value of 3490K. |
| **jeita_t6** | 0x24 | R/W | [15:0] | 4970 | Signed number that sets the JEITA temperature region transition temperature T6 between JEITA regions R6 and R7. The temperature is based on the thermistor reading from the telemetry system; RNTC = RNTCBIAS × (21829 - thermistor_voltage) / thermistor_voltage. Recall that the thermistor has a negative temperature coefficient so jeita_t1, representing colder temperatures, will have the highest value and jeita_t6, representing warmer temperatures, will have the lowest value. The default value of 4970 maps to about 60°C for the expected thermistor β value of 3490K. |
| **VCHARGE_ JEITA_6_5_REG** | 0x25 | R/W | [9:0] | 631 | vcharge_setting values for JEITA temperature regions jeita_t6 and jeita_t5 |
| vcharge_jeita_6 | | | [9:5] | 19 | Sets the charge voltage to be used in JEITA region 6 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to vcharge_setting and can be calculated using vcharge_jeita_6 × 12.5mV + 3.8125V. The default value of 19 corresponds to 4.05V. |
| vcharge_jeita_5 | | | [4:0] | 23 | Sets the charge voltage to be used in JEITA region 5 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to vcharge_setting and can be calculated using vcharge_jeita_5 × 12.5mV + 3.8125V. The default value of 23 corresponds to 4.1V. |
| **VCHARGE_ JEITA_4_3_2_REG** | 0x26 | R/W | [14:0] | 24575 | vcharge_setting values for JEITA temperature regions jeita_t4, jeita_t3, and jeita_t2 |
| vcharge_jeita_4 | | | [14:10] | 23 | Sets the charge voltage to be used in JEITA region 4 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to vcharge_setting and can be calculated using vcharge_jeita_4 × 12.5mV + 3.8125V. The default value of 23 corresponds to 4.1V |
| vcharge_jeita_3 | | | [9:5] | 31 | Sets the charge voltage to be used in JEITA region 3 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to vcharge_setting and can be calculated using vcharge_jeita_3 × 12.5mV + 3.8125V. The default value of 31 corresponds to 4.2V. |
| vcharge_jeita_2 | | | [4:0] | 31 | Sets the charge voltage to be used in JEITA region 2 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to vcharge_setting and can be calculated using vcharge_jeita_2 × 12.5mV + 3.8125V. The default value of 31 corresponds to 4.2V. |
| **ICHARGE_ JEITA_6_5_REG** | 0x27 | R/W | [9:0] | 495 | charge_current_setting values for JEITA temperature regions jeita_t6 and jeita_t5 |
| icharge_jeita_6 | | | [9:5] | 15 | Sets the charge current to be used in JEITA region 6 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to charge_current_setting where the charge current can be calculated using (icharge_jeita_6 + 1) × 1mV / RSNSB. The default value of 15 corresponds to a VCSP-VCSN servo voltage of 16mV which is half scale or C/2. |
| icharge_jeita_5 | | | [4:0] | 15 | Sets the charge current to be used in JEITA region 5 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to charge_current_setting where the charge current can be calculated using (icharge_jeita_5 + 1) × 1mV / RSNSB. The default value of 15 corresponds to a VCSP-VCSN servo voltage of 16mV which is half scale or C/2. |
| **ICHARGE_ JEITA_4_3_2_REG** | 0x28 | R/W | [14:0] | 32751 | charge_current_setting value for JEITA temperature regions jeita_t4, jeita_t3, and jeita_t2 |

# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| icharge_jeita_4 | | | [14:10] | 31 | Sets the charge current to be used in JEITA region 4 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to charge_current_setting where the charge current can be calculated using (icharge_jeita_4 + 1) × 1mV / RSNSB. The default value of 31 corresponds to a VCSP-VCSN servo voltage of 32mV which is full scale. |
| icharge_jeita_3 | | | [9:5] | 31 | Sets the charge current to be used in JEITA region 3 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to charge_current_setting where the charge current can be calculated using (icharge_jeita_3 + 1) × 1mV / RSNSB. The default value of 31 corresponds to a VCSP-VCSN servo voltage of 32mV which is full scale. |
| icharge_jeita_2 | | | [4:0] | 15 | Sets the charge current to be used in JEITA region 2 as illustrated in the JEITA Temperature Qualified Charging section. The value corresponds to charge_current_setting where the charge current can be calculated using (icharge_jeita_2 + 1) × 1mV / RSNSB. The default value of 15 corresponds to a VCSP-VCSN servo voltage of 16mV which is half scale or C/2. |
| **CHARGER_CONFIG_BITS_REG** | 0x29 | R/W | [2:0] | 1 | Battery charger configuration settings |
| en_c_over_x_term | | | [2] | 0 | Enables charge current based (C/x) battery charger termination as set by ibat dropping to the c_over_x_threshold in constant_voltage. |
| en_jeita | | | [0] | 1 | Enables the JEITA temperature qualified charging system. |
| **tchargetimer** | 0x30 | R | [15:0] | 0 | If max_charge_time is written to a non zero value tchargetimer is the elapsed time in minutes since the beginning of a charge cycle. The LTC4162 will terminate charging when tchargetimer reaches the value in max_charge_time. |
| **tcvtimer** | 0x31 | R | [15:0] | 0 | This is the elapsed time in seconds since the battery charger has been in the constant_voltage phase of charging. If this value exceeds max_cv_time then charging is considered complete and will terminate. |
| **charger_state** | 0x34 | R | [12:0] | 256 | Real time battery charger state indicator. Individual bits are mutually exclusive.<br>Enums: bat_detect_failed_fault = 4096,<br>battery_detection = 2048,<br>charger_suspended = 256,<br>precharge = 128,<br>cc_cv_charge = 64,<br>ntc_pause = 32,<br>timer_term = 16,<br>c_over_x_term = 8,<br>max_charge_time_fault = 4,<br>bat_missing_fault = 2,<br>bat_short_fault = 1 |
| **charge_status** | 0x35 | R | [5:0] | 0 | Charge status indicator. Individual bits are mutually exclusive and are only active in charging states.<br>Enums: ilim_reg_active = 32,<br>thermal_reg_active = 16,<br>vin_uvcl_active = 8,<br>iin_limit_active = 4,<br>constant_current = 2,<br>constant_voltage = 1,<br>charger_off = 0 |
| **LIMIT_ALERTS_REG** | 0x36 | R | [15:0] | 0 | Limit alert register. This input/output register indicates that an enabled alert has occurred. Individual alerts are enabled in EN_LIMIT_ALERTS_REG. Writing 0 to any bit clears that alert. Once set, alert bits remain high until cleared or disabled. |
| telemetry_valid_alert | | | [15] | 0 | Alert that indicates that the telemetry system warm-up time has expired and valid telemetry data is available from the serial port. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_telemetry_valid_alert. |

# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| bsr_done_alert | | | [14] | 0 | Alert that indicates that the battery equivalent-series-resistance measurement is finished and a result is available in bsr. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_bsr_done_alert. |
| vbat_lo_alert | | | [11] | 0 | Alert that indicates that vbat is below the value set by vbat_lo_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_vbat_lo_alert. |
| vbat_hi_alert | | | [10] | 0 | Alert that indicates that vbat is above the value set by vbat_hi_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_vbat_hi_alert. |
| vin_lo_alert | | | [9] | 0 | Alert that indicates that vin is below the value set by vin_lo_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_vin_lo_alert. |
| vin_hi_alert | | | [8] | 0 | Alert that indicates that vin is above the value set by vin_hi_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_vin_hi_alert. |
| vout_lo_alert | | | [7] | 0 | Alert that indicates that vout is below the value set by vout_lo_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_vout_lo_alert. |
| vout_hi_alert | | | [6] | 0 | Alert that indicates that vout is above the value set by vout_hi_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_vout_hi_alert. |
| iin_hi_alert | | | [5] | 0 | Alert that indicates that iin is above the value set by iin_hi_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_iin_hi_alert. |
| ibat_lo_alert | | | [4] | 0 | Alert that indicates that ibat is below the value set by ibat_lo_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_ibat_lo_alert. |
| die_temp_hi_alert | | | [3] | 0 | Alert that indicates that die_temp is above the value set by die_temp_hi_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_die_temp_hi_alert. |
| bsr_hi_alert | | | [2] | 0 | Alert that indicates that bsr is above the value set by bsr_hi_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_bsr_hi_alert. |
| thermistor_voltage_hi_alert | | | [1] | 0 | Alert that indicates that thermistor_voltage is above the value set by thermistor_voltage_hi_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_thermistor_voltage_hi_alert. |
| thermistor_voltage_lo_alert | | | [0] | 0 | Alert that indicates that thermistor_voltage is below the value set by thermistor_voltage_lo_alert_limit. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_thermistor_voltage_lo_alert. |
| **CHARGER_STATE_ALERTS_REG** | 0x37 | R | [12:0] | 0 | Alert that indicates that charger states have occurred. Individual bits are enabled by EN_CHARGER_STATE_ALERTS_REG. Writing 0 to any bit while writing 1s to the remaining bits clears that alert. Once set, alert bits remain high until cleared or disabled. |
| bat_detect_failed_fault_alert | | | [12] | 0 | Alert that indicates a bat_detect_failed_fault. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_bat_detect_failed_fault_alert. |
| battery_detection_alert | | | [11] | 0 | Alert that indicates the battery charger is performing battery_detection. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_battery_detecttion_alert. |
| charger_suspended_alert | | | [8] | 0 | Alert that indicates the battery charger is in the charger_suspended state. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_charger_suspended_alert. |

## REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| precharge_alert | | | [7] | 0 | Alert that indicates that the battery charger is in the precharge phase. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_precharge_alert. |
| cc_cv_charge_alert | | | [6] | 0 | Alert that indicates that the battery charge is in the cc_cv_charge phase. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_cc_cv_charge_alert. |
| ntc_pause_alert | | | [5] | 0 | Alert that indicates that the battery charger is in the ntc_pause state. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_ntc_pause_alert. |
| timer_term_alert | | | [4] | 0 | Alert that indicates that the battery charge is in the timer_term state. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_timer_term_alert. |
| c_over_x_term_alert | | | [3] | 0 | Alert that indicates that the battery charge is in the c_over_x_term state. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_c_over_x_term_alert. |
| max_charge_time_fault_alert | | | [2] | 0 | Alert that indicates that the battery charge is in the max_charge_time_fault state. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_max_charge_time_alert. |
| bat_missing_fault_alert | | | [1] | 0 | Alert that indicates that a bat_missing_fault has been detected. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_bat_missing_fault_alert. |
| bat_short_fault_alert | | | [0] | 0 | Alert that indicates that a bat_short_fault has been detected. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_bat_short_fault_alert. |
| **CHARGE_STATUS_ALERTS_REG** | 0x38 | R | [5:0] | 0 | Alerts that charge_status indicators have occurred. Individual bits are enabled by EN_CHARGE_STATUS_ALERTS_REG. Writing 0 to any bit clears that alert. Once set, alert bits remain high until cleared or disabled. |
| ilim_reg_active_alert | | | [5] | 0 | Alert that indicates that charge_status is ilim_reg_active. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_ilim_reg_active_alert. |
| thermal_reg_active_alert | | | [4] | 0 | Alert that indicates that charge_status is thermal_reg_active. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_thermal_reg_active_alert. |
| vin_uvcl_active_alert | | | [3] | 0 | Alert that indicates that charge_status is vin_uvcl_active. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_vin_uvcl_active_alert. |
| iin_limit_active_alert | | | [2] | 0 | Alert that indicates that charge_status is iin_limit_active. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_iin_limit_active_alert. |
| constant_current_alert | | | [1] | 0 | Alert that indicates that charge_status is constant_current. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_constant_current_alert. |
| constant_voltage_alert | | | [0] | 0 | Alert that indicates that charge_status is constant_voltage. This alert bit is cleared by writing it back to 0 with the remaining bits in this register set to 1s. It can also be cleared by clearing en_constant_voltage_alert. |
| **SYSTEM_STATUS_REG** | 0x39 | R | [8:0] | N/A | Real time system status indicator bits |
| en_chg | | | [8] | N/A | Indicates that the battery charger is active. |
| cell_count_err | | | [7] | N/A | A cell count error will occur and charging will be inhibited if the CELLS0 and CELLS1 pins are programmed for more than 8 cells. cell_count_err always indicates true when telemetry is not enabled such as when the charger is not enabled. |

# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| no_rt | | | [5] | N/A | Indicates that no frequency setting resistor is detected on the RT pin. The RT pin impedance detection circuit will typically indicate a missing RT resistor for values above 1.4MΩ. no_rt always indicates true when the battery charger is not enabled such as when there is no input power available. |
| thermal_shutdown | | | [4] | N/A | Indicates that the LTC4162 is in thermal shutdown protection due to an excessively high die temperature (typically 150°C). |
| vin_ovlo | | | [3] | N/A | Indicates that input voltage shutdown protection is active due to an input voltage above its protection shut-down threshold of approximately 38.6V. |
| vin_gt_vbat | | | [2] | N/A | Indicates that the VIN pin voltage is sufficiently above the battery voltage to begin a charge cycle (typically +150mV). |
| vin_gt_4p2v | | | [1] | N/A | Indicates that the VIN pin voltage is at least greater than the switching regulator under-voltage lockout level (4.2V typical). |
| intvcc_gt_2p8v | | | [0] | N/A | Indicates that the INTVCC pin voltage is greater than the telemetry system lockout level (2.8V typical). |
| **vbat** | 0x3A | R | [15:0] | 0 | Signed number that indicates the A/D measurement for the per-cell battery voltage. The value is based on the A/D scaling factor for the battery voltage measurement which is cell_count × 192.4µV/LSB at the BATSENS+ pin. |
| **vin** | 0x3B | R | [15:0] | 0 | Signed number that indicates the A/D measurement for the input voltage. The value is based on the A/D scaling factor for the input voltage measurement which is 1.649mV/LSB. |
| **vout** | 0x3C | R | [15:0] | 0 | Signed number that indicates the A/D measurement for the vout voltage. The value is based on the A/D scaling factor for the output voltage measurement which is 1.653mV/LSB. |
| **ibat** | 0x3D | R | [15:0] | 0 | Signed number that indicates the A/D measurement for the battery current. The value is based on the A/D scaling factor for the charge current measurement (VCSP - VCSN) which is 1.466µV / RSNSB amperes/LSB. If the charger is not enabled the value represents drain on the battery and will be negative. |
| **iin** | 0x3E | R | [15:0] | 0 | Signed number that indicates the A/D measurement for the input current (VCLP - VCLN). The value is based on the A/D scaling factor for the input current measurement which is 1.466µV / RSNSI amperes/LSB. |
| **die_temp** | 0x3F | R | [15:0] | 0 | Signed number that indicates the A/D measurement for the die temperature. The value can be calculated from the A/D reading in °C as TDIE(°C) = die_temp × 0.0215°C/LSB - 264.4°C. |
| **thermistor_voltage** | 0x40 | R | [15:0] | 0 | Signed number that indicates the A/D measurement for the NTC pin voltage. The thermistor value can be determined by the expression RNTC = RNTCBIAS × thermistor_voltage / (21829 - thermistor_voltage). Recall that the thermistor has a negative temperature coefficient so higher temperatures make lower thermistor_voltage readings and vice-versa. Enum: open_thermistor = 21684 |
| **bsr** | 0x41 | R | [15:0] | 0 | Indicates the A/D measurement for the per-cell battery resistance. The battery resistance is relative to the battery charge current setting resistor, RSNSB, and can be computed in Ω from cell_count × bsr × RSNSB / 500. If the charge current, ibat, is below icharge_over_10, bsr_questionable will be set. |

## REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| **jeita_region** | 0x42 | R | [2:0] | 0 | Indicates the LTC4162 JEITA battery temperature region containing the thermistor_voltage. The temperature region consists of the values bounded by the transition temperatures jeita_t(R-1) and jeita_t(R). Recall that the thermistor has a negative temperature coefficient so higher temperatures make lower thermistor_voltage readings and vice-versa. JEITA temperature-controlled charging is active only when en_jeita is at its default value of 1. JEITA regions R7 (jeita_region = 7) and R1 (jeita_region = 1) indicate that the thermistor_voltage (battery temperature) is out of range for charging and therefore charging is paused (ntc_pause). The transition temperatures are set by jeita_t1 through jeita_t6.<br>Enums: R7 = 7,<br>R6 = 6,<br>R5 = 5,<br>R4 = 4,<br>R3 = 3,<br>R2 = 2,<br>R1 = 1 |
| **CHEM_CELLS_REG** | 0x43 | R | [11:0] | 0 | Programmed battery chemistry |
| chem | | | [11:8] | 0 | Indicates the chemistry of the battery being charged. For additional safety, application software can test this value to ensure that the correct version of the LTC4162 (LTC4162-L, LTC4162-F or LTC4162-S) is populated on the circuit board.<br>Enums: LTC4162_LAD = 0,<br>LTC4162_L42 = 1,<br>LTC4162_L41 = 2,<br>LTC4162_L40 = 3,<br>LTC4162_FAD = 4,<br>LTC4162_FFS = 5,<br>LTC4162_FST = 6,<br>LTC4162_SST = 8,<br>LTC4162_SAD = 9 |
| cell_count | | | [3:0] | 0 | Indicates the cell count value detected by the CELLS0 and CELLS1 pin strapping. cell_count always indicates 0 when the battery charger is not enabled such as when there is no input power available.<br>Enum: Unknown = 0 |
| **icharge_dac** | 0x44 | R | [4:0] | 0 | Indicates the actual charge current setting applied to the charge current digital to analog converter. icharge_dac is ramped up/down to implement digital soft-start/stop. The LTC4162 sets the value of icharge_dac based on charger_state, thermistor_voltage, and charger settings including charge_current_setting, icharge_jeita_2 through icharge_jeita_6, jeita_t1 through jeita_t6 and en_jeita. Recall that the charge current is regulated by controlling the voltage across an external current sense resistor RSNSB. The servo voltage is given by (icharge_dac + 1) × 1mV. The charge current servo level is thus given by (icharge_dac + 1) × 1mV/RSNSB. |
| **vcharge_dac** | 0x45 | R | [4:0] | 0 | This is the actual battery voltage setting applied to the charge voltage digital to analog converter. The LTC4162 sets the value of vcharge_dac based on charger_state, thermistor_voltage, and charger settings including vcharge_setting, vcharge_jeita_2 through vcharge_jeita_6, jeita_t1 through jeita_t6, thermistor_voltage and en_jeita. The charge voltage setting can be computed from cell_count × (vcharge_setting × 12.5mV + 3.8125V) where vcharge_setting ranges from 0 to 31 (4.2V max). |
| **iin_limit_dac** | 0x46 | R | [5:0] | 0 | Indicates the actual input current limit. The iin_limit_dac will follow the value programmed in iin_limit_target. The input current will be regulated to a maximum value given by (iin_limit_dac + 1) × 500µV / RSNSI. |
| **vbat_filt** | 0x47 | R | [15:0] | 0 | Signed number that is a digitally filtered version of the A/D measurement of vbat. The value is based on the A/D scaling factor for the battery voltage measurement which is cell_count × 192.4µV/LSB at the BATSENS+ pin. |

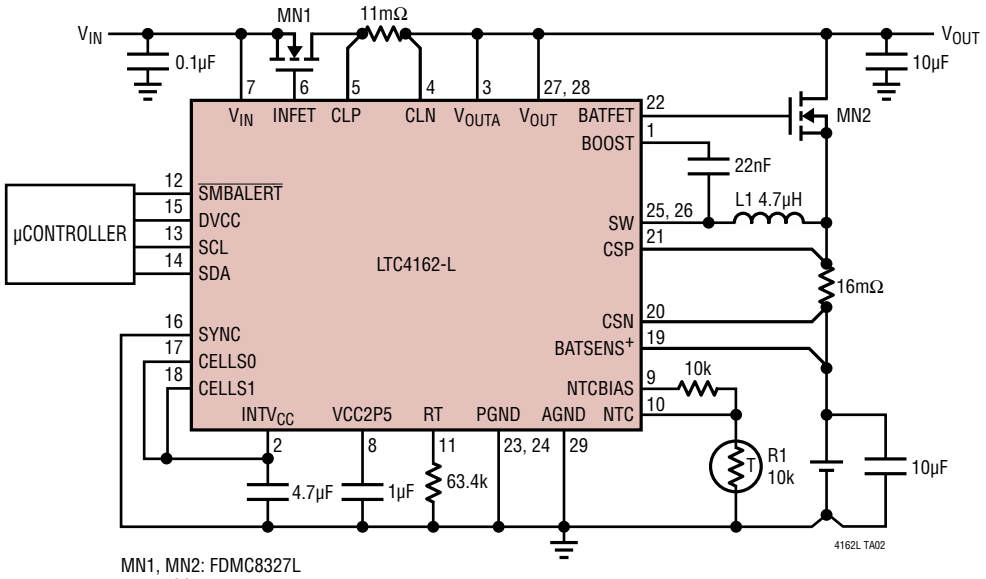
# REGISTER DESCRIPTIONS

| Symbol Name | Command Code | Access | Bit Range | Default | Description |
|---|---|---|---|---|---|
| **bsr_charge_current** | 0x48 | R | [15:0] | 0 | Signed number that is the battery charge current that existed during the battery series resistance measurement. The value is based on the A/D value, ibat, which has a scaling factor of 1.466µV / RSNSB amperes/LSB. If the battery series resistance (bsr) test runs with ibat values less than icharge_over_10, the accuracy of the test is questionable due to low signal level and bsr_questionable will set. Rerunning the battery series resistance test earlier in the charge cycle with higher ibat, and therefore higher bsr_charge_current, will give the most accurate result.<br>Enum: icharge_over_10 = 2184 |
| **TELEMETRY_ STATUS_REG** | 0x4A | R | [1:0] | 0 | Telemetry system status register |
| bsr_questionable | | | [1] | 0 | Indicates that the battery series resistance measurement is questionable due to low signal, specifically that ibat was less than icharge_over_10, when the last battery series resistance (bsr) measurement was taken. bsr_charge_current contains the ibat A/D value present when the battery series resistance measurement was made. |
| telemetry_valid | | | [0] | 0 | Indicates that the telemetry system autozero amplifiers have had sufficient time, approximately 12ms, to null their offsets. Battery charging is disabled until the telemetry system warm up time has passed. |
| **input_undervoltage_ dac** | 0x4B | R | [7:0] | 0 | Input undervoltage regulation digital to analog converter value. The regulation voltage is given by (input_undervoltage_dac + 1) × 140.625mV. If enabled, the MPPT algorithm will directly manipulate this value. Otherwise it will follow input_undervoltage_setting. |

Revision: 1773 Date: 2018-03-15 22:40:27 -0400 (Thu, 15 Mar 2018)

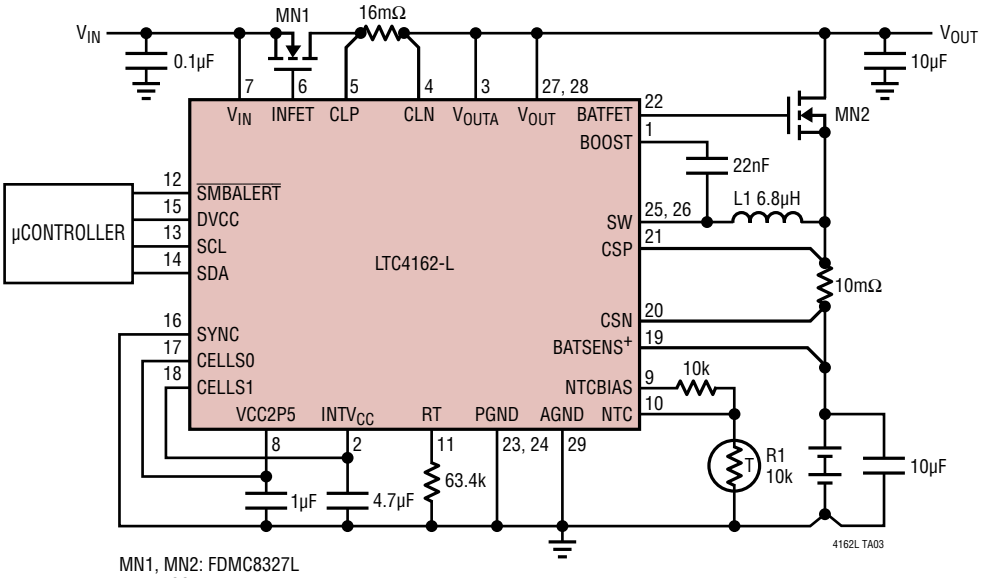
# TYPICAL APPLICATIONS

### 1-Cell USB Power Delivery Charger with PowerPath




MN1, MN2: FDMC8327L
R1: NTCS0402E3103FLT
L1: XAL5030-472MEC

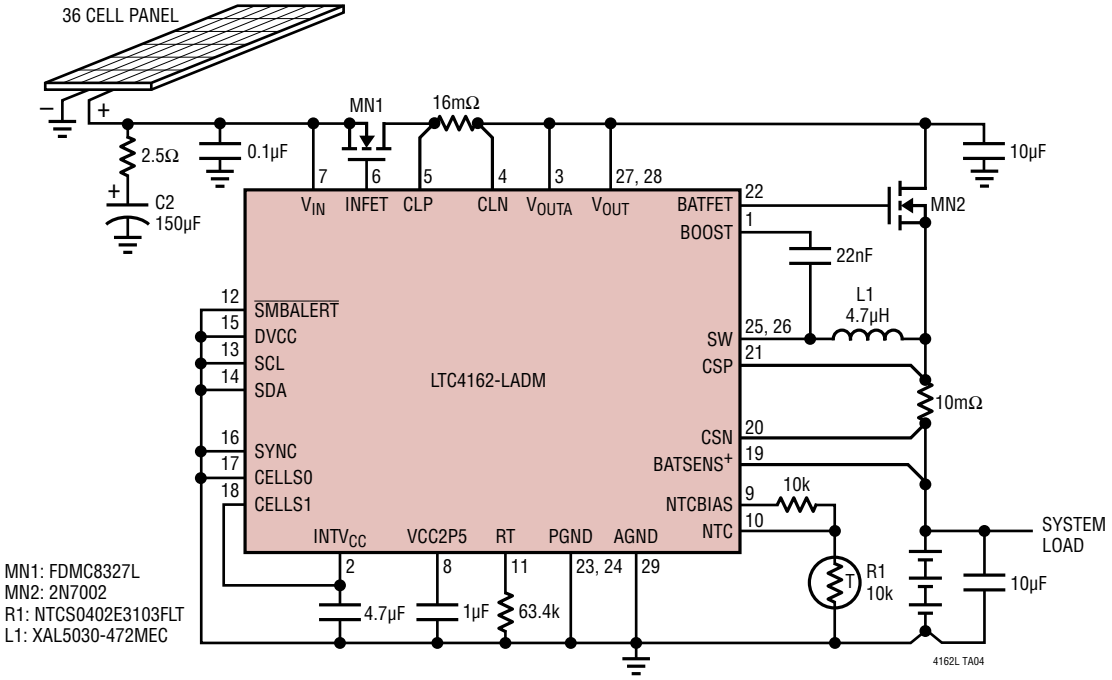
### 9V to 35V 2-Cell 3.2A Charger with PowerPath and 2A Input Limit




MN1, MN2: FDMC8327L
R1: NTCS0402E3103FLT
L1: XAL6060-682MEC

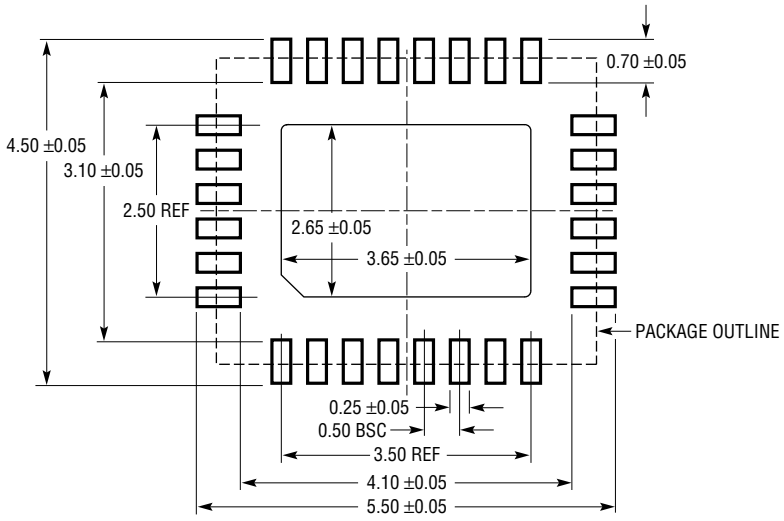
# TYPICAL APPLICATIONS

**Solar Powered 3-Cell 3.2A Charger with Maximum Power Point Tracking**

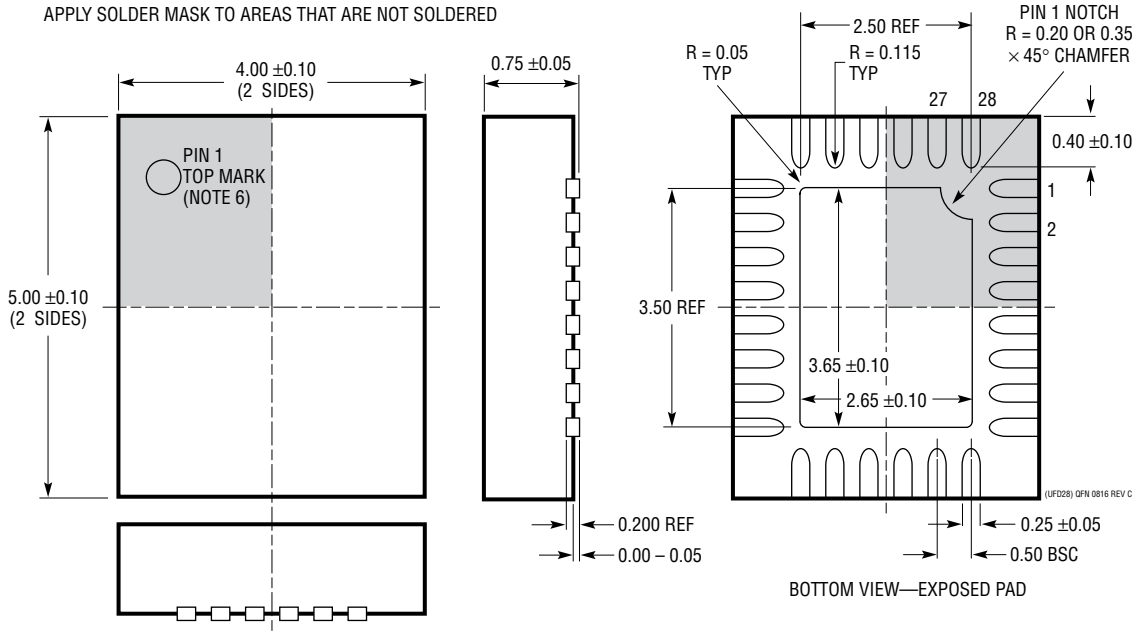


# PACKAGE DESCRIPTION

**UFD Package**
**28-Lead Plastic QFN (4mm × 5mm)**
(Reference LTC DWG # 05-08-1712 Rev C)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 10/18 | Changed Parameter and Conditions for Symbol $V_{OLI2C}$ | 6 |
| | | Changed 3.5µA to 2.8µA in Low Power Ship Mode section | 28 |



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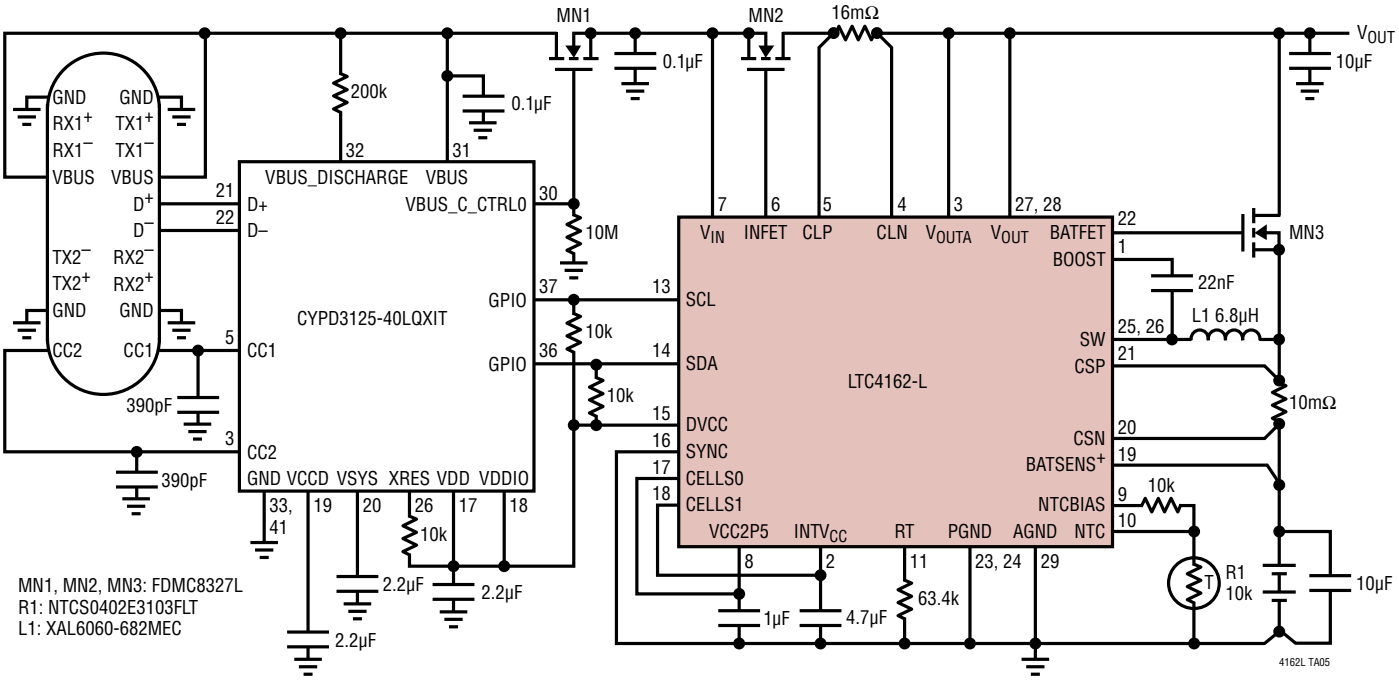
## TYPICAL APPLICATION

**USB PD (C Cable) Based Battery Charger with Power Path**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC4015 | Multichemistry Buck Battery Charger Controller with Digital Telemetry System | Multichemistry Li-Ion/Polymer, LiFePO4, or Lead-Acid Synchronous Buck Battery Charger with Termination; High Efficiency; Digital Telemetry System Monitors $V_{BTA}$, $I_{BAT}$, $R_{BAT}$, NTC Ratio (Battery Temperature), $V_{IN}$, $I_{IN}$, $V_{SYSTEM}$, Die Temperature; Coulomb Counter and Integrated 14-Bit ADC; Charging Input Voltage Range: 4.5V to 35V; Battery Voltage Range: Up to 35V; MPPT; 4mm × 5mm QFN-28 Package |
| LT3651-4.X/ LT3651-8.X | Monolithic 4A Switch Mode Synchronous 1-Cell Li-Ion Battery Charger | Standalone, 4.75V ≤ $V_{IN}$ ≤ 32V (40V Abs Max), 1MHz, 4A, Programmable Charge Current Timer or C/10 Termination, 5mm × 6mm QFN-36 Package |
| LT3652/LT3652HV | Power Tracking 2A Buck Battery Charger | Input Supply Voltage Regulation Loop for Peak Power Tracking in (MPPT) Solar Applications, Standalone, 4.95V ≤$V_{IN}$ ≤ 32V (40V Abs Max), 1MHz Timer or C/10 Termination, 3mm × 3mm DFN-12 Package and MSOP-12 Packages, LT3652HV Version Up to $V_{IN}$ = 34V |
| LTC4012/LTC4012-1/ LTC4012-2/ LTC4012-3 | 4A, High Efficiency, Multi-Chemistry Battery Charger with PowerPath Control | PowerPath Control, Resistor Voltage/Current Programming, 1-to 4-Cell Li, Up to 18-Cell Ni, SLA and Supercap Compatible; 4mm × 4mm QFN-20 Package, –1 Version for 4.1V Li Cells, –2 Version for 4.2V Li Cells, –3 Version Has Extra GND Pin |
| LTC4020 | 55V Buck-Boost Multi-Chemistry Battery Charger | Constant-Current/Constant-Voltage Buck-Boost Switching Controller Regulator Charger, 5mm × 7mm QFN-38 Package |
| LTC4121/ LTC4121-4.2 | Multi-Chemistry Buck Battery Charger | Constant-Current/Constant-Voltage 400mA Monolithic Buck Switching Regulator Charger, 4.4V ≤ $V_{IN}$ ≤ 40V, 3mm × 3mm QFN-16 Package |
| LTC4155 | Dual Input Power Manager/3.5A Li-Ion Battery Charger | High Efficiency, Monolithic Switching Regulator, 4mm × 5mm QFN-28 Package |
| LT8490 | High Voltage, High Current Buck-Boost Charge Controller with Maximum Power Point Tracking (MPPT) | Buck-Boost Switching Regulator Battery Charger that Implements a Constant-Current Constant-Voltage (CCCV) Charging Profile Used for Most Battery Types, Including Sealed Lead-Acid (SLA), Flooded, Gel and Lithium-Ion |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Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9