

TSOP, FP-BGA  
Commercial Temp  
Industrial Temp

## 64K x 16 1Mb Asynchronous SRAM

7, 8, 10, 12 ns  
3.3 V  $V_{DD}$   
Center  $V_{DD}$  and  $V_{SS}$

### Features

- Fast access time: 7, 8, 10, 12 ns
- CMOS low power operation: 145/125/100/85 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Byte control
- Fully static operation
- Industrial Temperature Option:  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- Package line up
  - GP: RoHS-compliant 400 mil, 44-pin TSOP Type II package
  - U: 6 mm x 8 mm Fine Pitch Ball Grid Array package
  - GU: RoHS-compliant 6 mm x 8 mm Fine Pitch Ball Grid Array package

### Description

The GS71116A is a high speed CMOS static RAM organized as 65,536-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS71116A is available in the 6 mm x 8 mm Fine Pitch BGA and 400 mil TSOP Type-II packages.

### Pin Descriptions

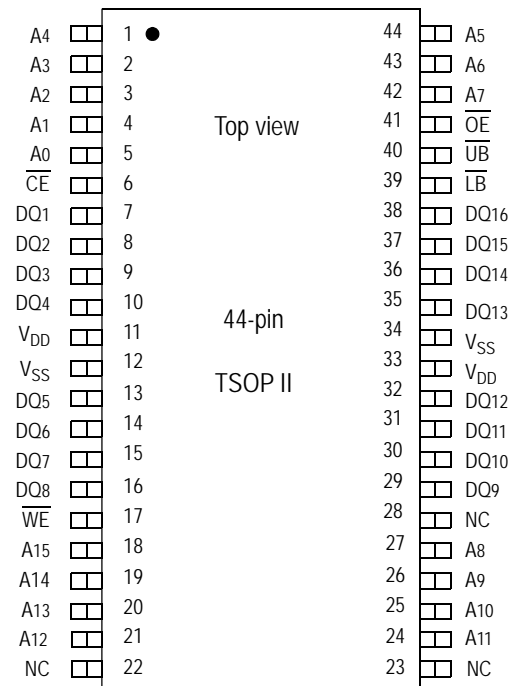
Symbol	Description
$A_0$ – $A_{15}$	Address input
$DQ_1$ – $DQ_{16}$	Data input/output
$\overline{CE}$	Chip enable input
$\overline{LB}$	Lower byte enable input (DQ1 to DQ8)
$\overline{UB}$	Upper byte enable input (DQ9 to DQ16)
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
$V_{DD}$	+3.3 V power supply
$V_{SS}$	Ground
NC	No connect

### Fine Pitch BGA 64K x 16-Bump Configuration

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	$A_0$	$A_1$	$A_2$	NC
B	$DQ_{16}$	$\overline{UB}$	$A_3$	$A_4$	$\overline{CE}$	$DQ_1$
C	$DQ_{14}$	$DQ_{15}$	$A_5$	$A_6$	$DQ_2$	$DQ_3$
D	$V_{SS}$	$DQ_{13}$	NC	$A_7$	$DQ_4$	$V_{DD}$
E	$V_{DD}$	$DQ_{12}$	NC	NC	$DQ_5$	$V_{SS}$
F	$DQ_{11}$	$DQ_{10}$	$A_8$	$A_9$	$DQ_7$	$DQ_6$
G	$DQ_9$	NC	$A_{10}$	$A_{11}$	$\overline{WE}$	$DQ_8$
H	NC	$A_{12}$	$A_{13}$	$A_{14}$	$A_{15}$	NC

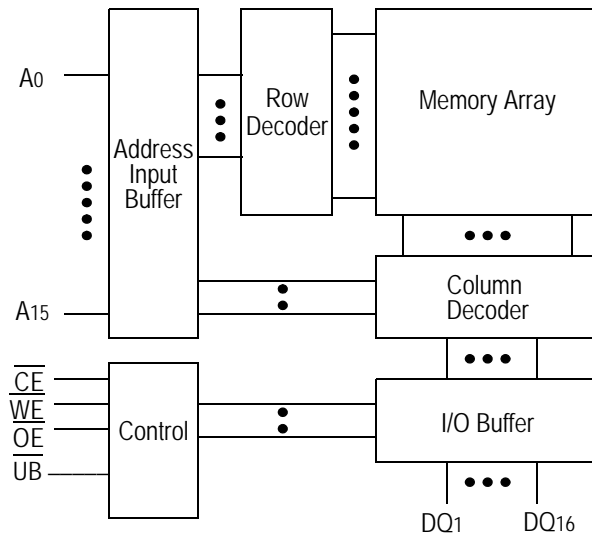
6 mm x 8 mm, 0.75 mm Bump Pitch (Package U)  
Top View

### TSOP-II 64K x 16-Pin Configuration



Package TP

## Block Diagram



## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ1 to DQ8	DQ9 to DQ16	$V_{DD}$ Current
H	X	X	X	X	Not Selected	Not Selected	ISB1, ISB2
L	L	H	L	L	Read	Read	I <sub>DD</sub>
			L	H	Read	High Z	
			H	L	High Z	Read	
L	X	L	L	L	Write	Write	
			L	H	Write	Not Write, High Z	
			H	L	Not Write, High Z	Write	
L	H	H	X	X	High Z	High Z	
L	X	X	H	H	High Z	High Z	

## Note:

X: "H" or "L"

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{DD}$	-0.5 to +4.6	V
Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
Output Voltage	$V_{OUT}$	-0.5 to $V_{DD} + 0.5$ ( $\leq 4.6$ V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	$T_{STG}$	-55 to 150	$^{\circ}C$

**Note:**

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

### Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -7/-8/-10/-12	$V_{DD}$	3.0	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	$T_{Ac}$	0	—	70	$^{\circ}C$
Ambient Temperature, Industrial Range	$T_{AI}$	-40	—	85	$^{\circ}C$

**Notes:**

1. Input overshoot voltage should be less than  $V_{DD} + 2$  V and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

### Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0$ V	5	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0$ V	7	pF

**Notes:**

1. Tested at  $T_A = 25^{\circ}C$ ,  $f = 1$  MHz
2. These parameters are sampled and are not 100% tested.

## DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	$I_{IL}$	$V_{IN} = 0 \text{ to } V_{DD}$	-1 $\mu\text{A}$	1 $\mu\text{A}$
Output Leakage Current	$I_{LO}$	Output High Z $V_{OUT} = 0 \text{ to } V_{DD}$	-1 $\mu\text{A}$	1 $\mu\text{A}$
Output High Voltage	$V_{OH}$	$I_{OH} = -4 \text{ mA}$	2.4	
Output Low Voltage	$V_{OL}$	$I_{LO} = +4 \text{ mA}$		0.4V

## Power Supply Currents

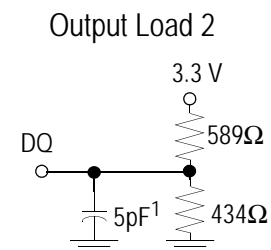
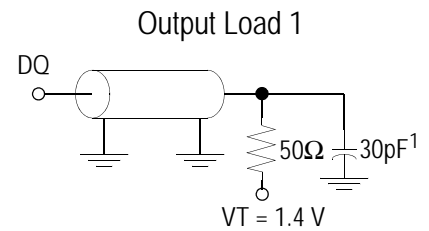
Parameter	Symbol	Test Conditions	0 to 70°C				-40 to 85°C			
			7 ns	8 ns	10 ns	12 ns	7 ns	8 ns	10 ns	12 ns
Operating Supply Current	$I_{DD}$	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0 \text{ mA}$	145 mA	125 mA	100 mA	85 mA	150 mA	130 mA	105 mA	90 mA
Standby Current	$I_{SB1}$	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	25 mA	20 mA	20 mA	15 mA	30 mA	25 mA	25 mA	20 mA
Standby Current	$I_{SB2}$	$\overline{CE} \geq V_{DD} - 0.2 \text{ V}$ All other inputs $\geq V_{DD} - 0.2 \text{ V}$ or $\leq 0.2 \text{ V}$	2 mA				5 mA			

## AC Test Conditions

Parameter	Conditions
Input high level	$V_{IH} = 2.4 \text{ V}$
Input low level	$V_{IL} = 0.4 \text{ V}$
Input rise time	$t_r = 1 \text{ V/ns}$
Input fall time	$t_f = 1 \text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	Fig. 1 & 2

**Notes:**

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$



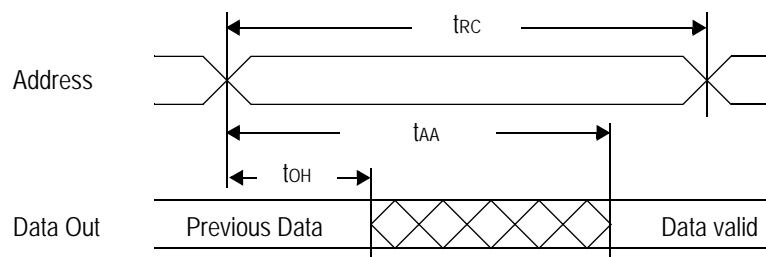
## AC Characteristics

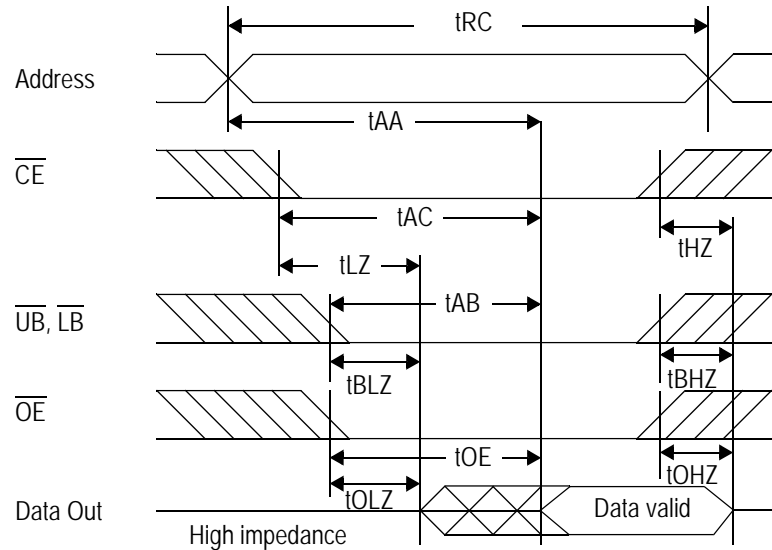
## Read Cycle

Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	7	—	8	—	10	—	12	—	ns
Address access time	$t_{AA}$	—	7	—	8	—	10	—	12	ns
Chip enable access time ( $\overline{CE}$ )	$t_{AC}$	—	7	—	8	—	10	—	12	ns
Byte enable access time ( $\overline{UB}$ , $\overline{LB}$ )	$t_{AB}$	—	3	—	3.5	—	4	—	5	ns
Output enable to output valid ( $\overline{OE}$ )	$t_{OE}$	—	3	—	3.5	—	4	—	5	ns
Output hold from address change	$t_{OH}$	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	$t_{LZ}^*$	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	$t_{OLZ}^*$	0	—	0	—	0	—	0	—	ns
Byte enable to output in low Z ( $\overline{UB}$ , $\overline{LB}$ )	$t_{BLZ}^*$	0	—	0	—	0	—	0	—	ns
Chip disable to output in High Z ( $\overline{CE}$ )	$t_{HZ}^*$	—	3.5	—	4	—	5	—	6	ns
Output disable to output in High Z ( $\overline{OE}$ )	$t_{OHZ}^*$	—	3	—	3.5	—	4	—	5	ns
Byte disable to output in High Z ( $\overline{UB}$ , $\overline{LB}$ )	$t_{BHZ}^*$	—	3	—	3.5	—	3.5	—	3.5	—

\* These parameters are sampled and are not 100% tested.

Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ ,  $\overline{UB}$  and, or  $\overline{LB} = V_{IL}$

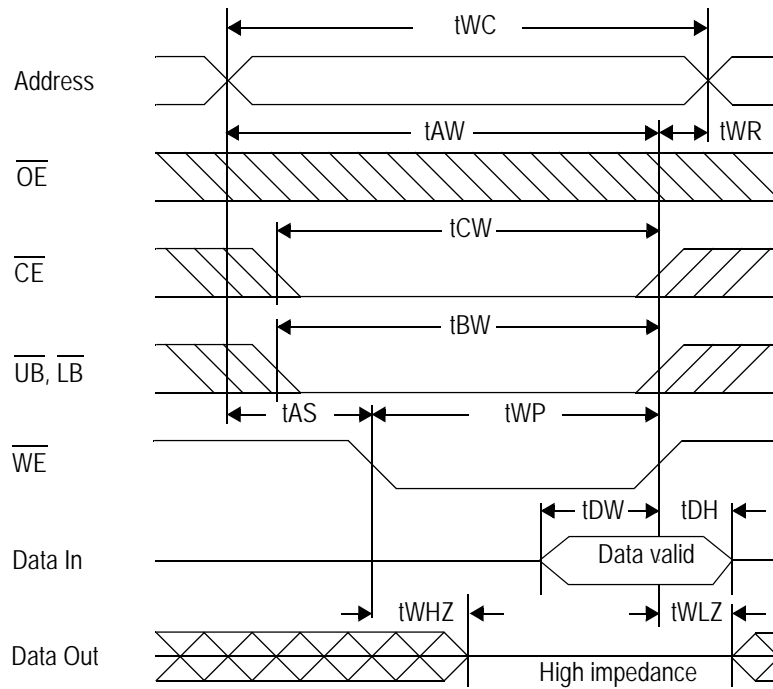
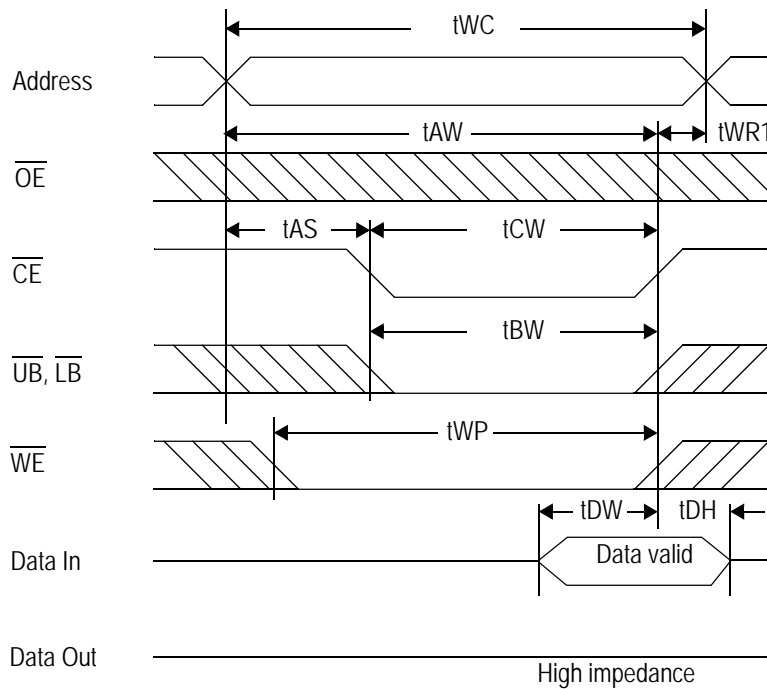


Read Cycle 2:  $\overline{WE} = V_{IH}$ 


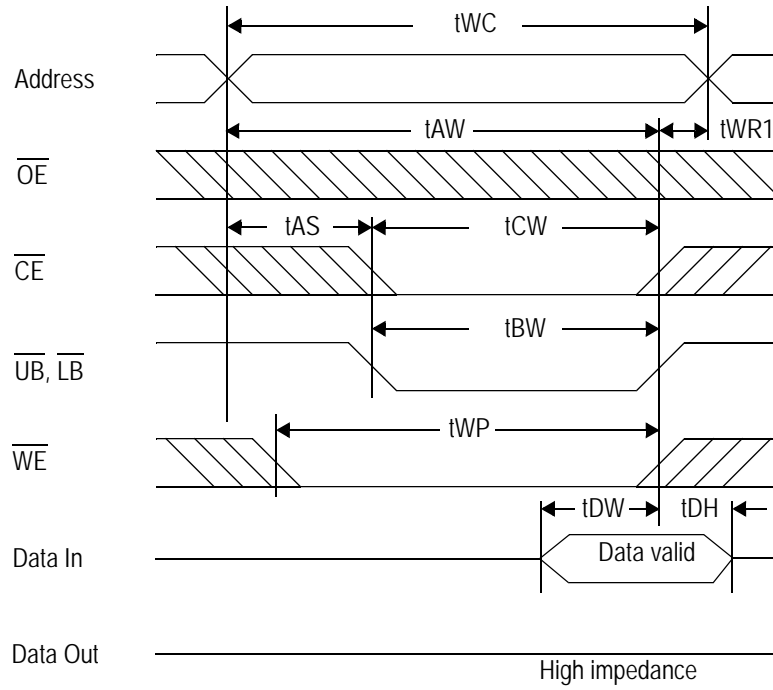
## Write Cycle

Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	7	—	8	—	10	—	12	—	ns
Address valid to end of write	$t_{AW}$	5	—	5.5	—	7	—	8	—	ns
Chip enable to end of write	$t_{CW}$	5	—	5.5	—	7	—	8	—	ns
Byte enable to end of write	$t_{BW}$	5	—	5.5	—	7	—	8	—	ns
Data set up time	$t_{DW}$	3.5	—	4	—	5	—	6	—	ns
Data hold time	$t_{DH}$	0	—	0	—	0	—	0	—	ns
Write pulse width	$t_{WP}$	5	—	5.5	—	7	—	8	—	ns
Address set up time	$t_{AS}$	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	$t_{WR}$	0	—	0	—	0	—	0	—	ns
Write recovery time ( $\overline{CE}$ )	$t_{WR1}$	0	—	0	—	0	—	0	—	ns
Output Low Z from end of write	$t_{WLZ}^*$	3	—	3	—	3	—	3	—	ns
Write to output in High Z	$t_{WHZ}^*$	—	3	—	3.5	—	4	—	5	ns

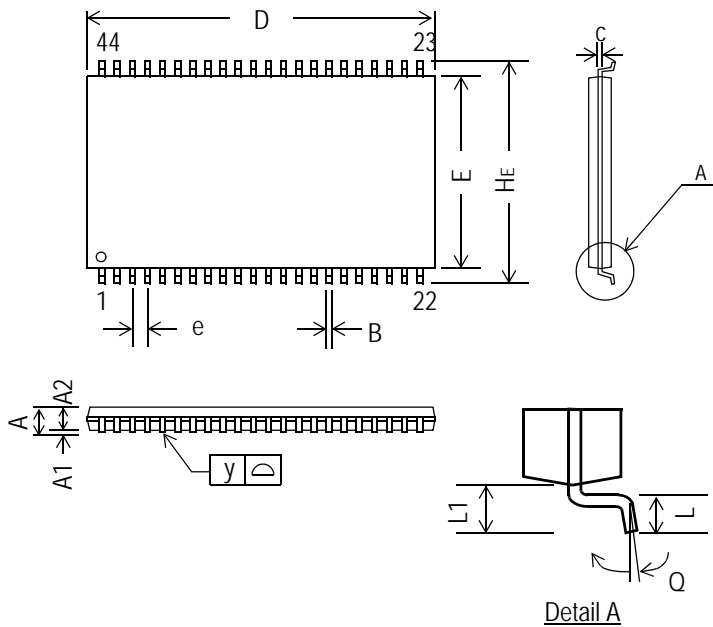
\* These parameters are sampled and are not 100% tested.

Write Cycle 1:  $\overline{WE}$  control

 Write Cycle 2:  $\overline{CE}$  control




Write Cycle 3:  $\overline{UB}$ ,  $\overline{LB}$  control


## 44 Pin, 400 mil TSOP-II

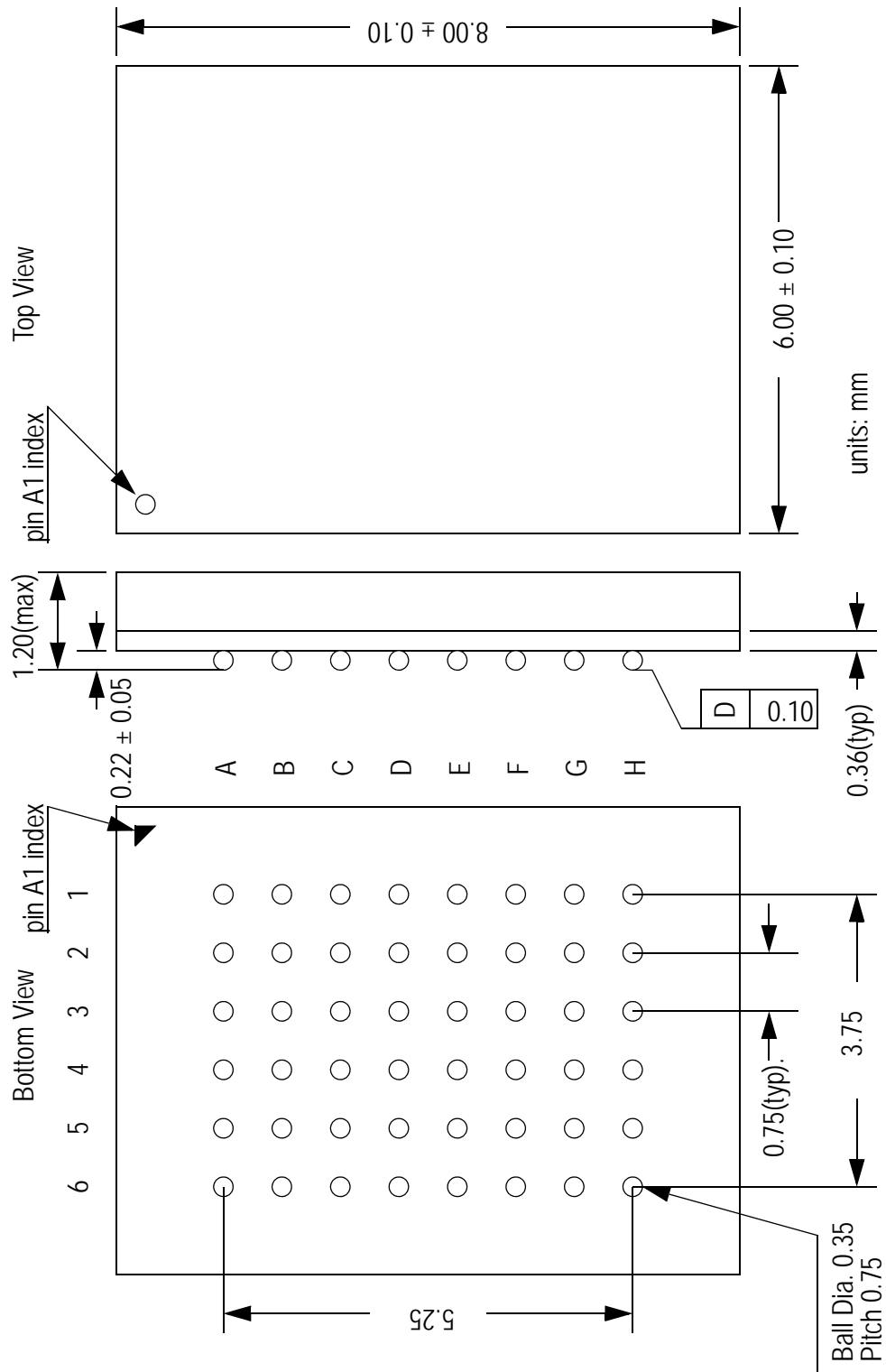


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.047	—	—	1.20
A1	0.002	—	—	0.05	—	—
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	—	0.006	—	—	0.15	—
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	—	0.031	—	—	0.80	—
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	—	0.031	—	—	0.80	—
y	—	—	0.004	—	—	0.10
Q	0°	—	5°	0°	—	5°

**Notes:**

1. Dimension D & E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm

## 6 mm x 8 mm Fine Pitch BGA



**Ordering Information**

Part Number *	Package	Access Time	Temp. Range
GS71116AGP-7	RoHS-compliant 400 mil TSOP-II	7 ns	Commercial
GS71116AGP-8	RoHS-compliant 400 mil TSOP-II	8 ns	Commercial
GS71116AGP-10	RoHS-compliant 400 mil TSOP-II	10 ns	Commercial
GS71116AGP-12	RoHS-compliant 400 mil TSOP-II	12 ns	Commercial
GS71116AGP-7I	RoHS-compliant 400 mil TSOP-II	7 ns	Industrial
GS71116AGP-8I	RoHS-compliant 400 mil TSOP-II	8 ns	Industrial
GS71116AGP-10I	RoHS-compliant 400 mil TSOP-II	10 ns	Industrial
GS71116AGP-12I	RoHS-compliant 400 mil TSOP-II	12 ns	Industrial
GS71116AU-7	6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial
GS71116AU-8	6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial
GS71116AU-10	6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial
GS71116AU-12	6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial
GS71116AU-7I	6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial
GS71116AU-8I	6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial
GS71116AU-10I	6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial
GS71116AU-12I	6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial
GS71116AGU-7	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial
GS71116AGU-8	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial
GS71116AGU-10	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial
GS71116AGU-12	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial
GS71116AGU-7I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial
GS71116AGU-8I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial
GS71116AGU-10I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial
GS71116AGU-12I	RoHS-compliant 6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial

**Note:**

Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS71116AGP-8T.

## 1Mb Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Revision
71116A_r1		<ul style="list-style-type: none"> <li>• Creation of new datasheet</li> </ul>
71116A_r1; 71116_r1_01	Content	<ul style="list-style-type: none"> <li>• Added 6 ns speed bin to entire document</li> </ul>
71116A_r1_01; 71116A_r1_02	Content	<ul style="list-style-type: none"> <li>• Updated all power numbers</li> <li>• Changed 6 mm x 10 mm FPBGA package designator from U to X</li> </ul>
71116A_r1_02; 71116A_r1_03	Content	<ul style="list-style-type: none"> <li>• Updated Recommended Operating Conditions table on page 4</li> <li>• Changed FPBGA package from 6 x 10 to 6 x 8 (package U)</li> <li>• Updated Read Cycle AC Characteristics table</li> </ul>
71116A_r1_03; 71116A_r1_04	Content	<ul style="list-style-type: none"> <li>• Removed 6 ns speed bin from entire document</li> <li>• Added 7 ns speed bin to entire document</li> </ul>
71116A_r1_04; 71116A_r1_05	Content	<ul style="list-style-type: none"> <li>• Updated timings for tBHZ (Read Cycle) for 10 ns and 12 ns</li> </ul>
71116A_r1_05; 71116A_r1_06	Content/Format	<ul style="list-style-type: none"> <li>• Updated format</li> <li>• Added RoHS-compliant information for TSOP-II package</li> </ul>
71116A_r1_06; 71116A_r1_07	Content/Format	<ul style="list-style-type: none"> <li>• Added RoHS-compliant information for FP-BGA package</li> </ul>
71116A_r1_07; 71116A_r1_08	Content	<ul style="list-style-type: none"> <li>• Added RoHS-compliant 400 mil SOJ</li> </ul>
71116A_r1_08; 71116A_r1_09	Content	<ul style="list-style-type: none"> <li>• Updated to MP in ordering information table</li> <li>• Rev.1.09a Removed Status column from Ordering Information table.</li> <li>• Removed reference to 400 mil, 44-pin SOJ package from entire document</li> </ul>
71116A_r1_09; 71116A_r1_10	Content	<ul style="list-style-type: none"> <li>• Removed 5/6-RoHS TSOP-II references due to EOL</li> </ul>

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