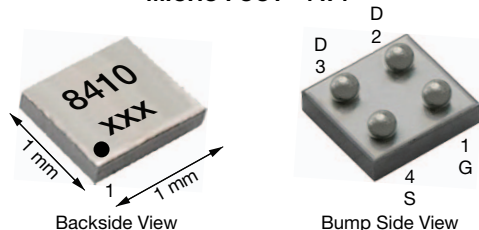


N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^a	Q _g (TYP.)
20	0.037 at V _{GS} = 4.5 V	5.7	5.9 nC
	0.041 at V _{GS} = 2.5 V	5.4	
	0.047 at V _{GS} = 1.8 V	5.0	
	0.068 at V _{GS} = 1.5 V	4.2	

MICRO FOOT® 1 x 1



Marking Code: 8410

Ordering Information:

Si8410DB-T2-E1 (Lead (Pb)-free and Halogen-free)

FEATURES

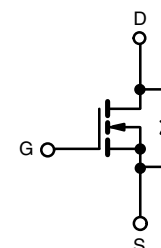
- TrenchFET® power MOSFET
- Ultra small 1 mm x 1 mm maximum outline
- Ultra-thin 0.54 mm maximum height
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch
- Power management
- High speed switching



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _A = 25 °C	A
		T _A = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current (t = 100 μs)	I _{DM}	20	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	0.65 ^c
Maximum Power Dissipation	P _D	T _A = 25 °C	W
		T _A = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Package Reflow Conditions ^e	VPR	260	
	IR/Convection	260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{a, b}	R _{thJA}	55	70	°C/W
Maximum Junction-to-Ambient ^{c, d}		125	160	

Notes

- Surface mounted on 1" x 1" FR4 board with full copper, t = 10 s, T_A = 25 °C.
- Maximum under steady state conditions is 100 °C/W.
- Surface mounted on 1" x 1" FR4 board with minimum copper, t = 10 s.
- Maximum under steady state conditions is 190 °C/W.
- Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
- In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.

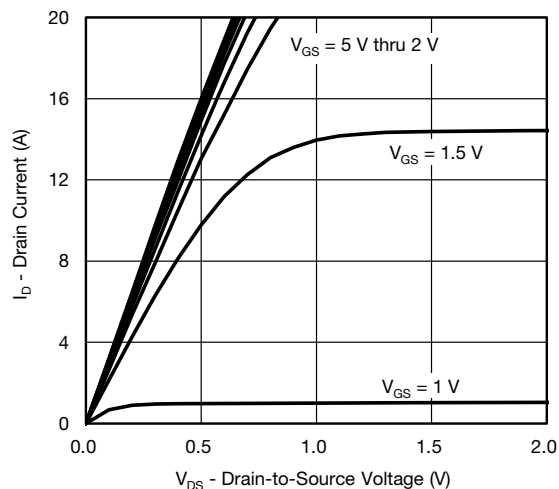
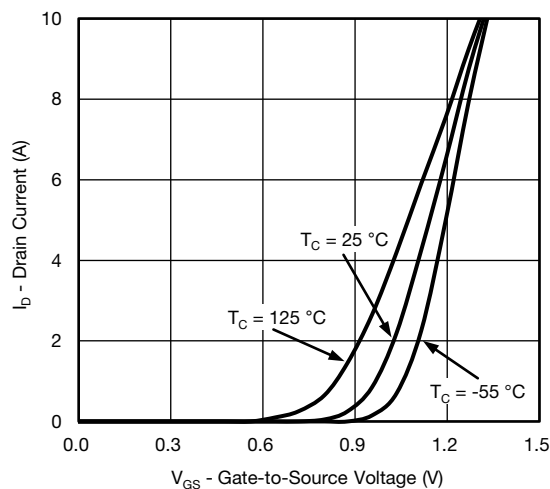
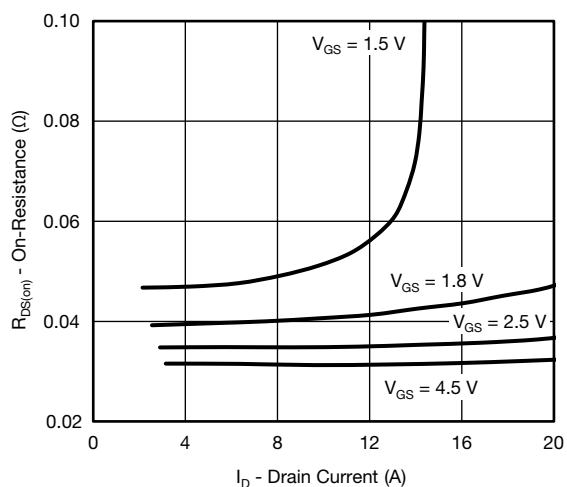
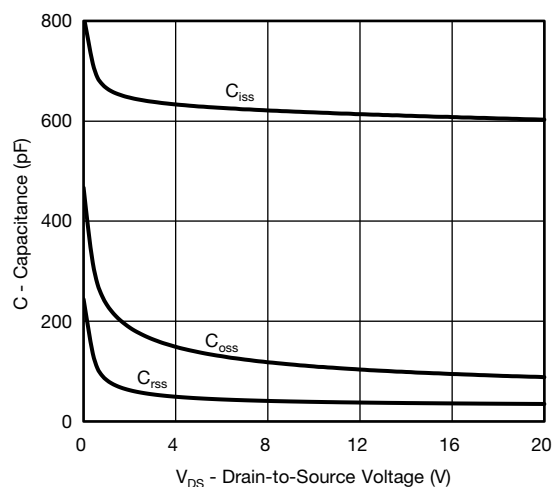
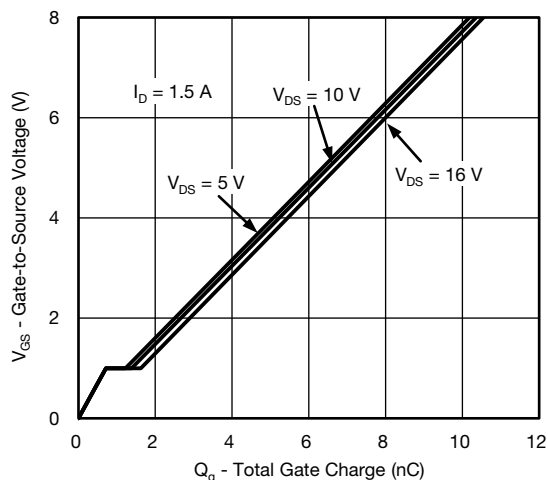
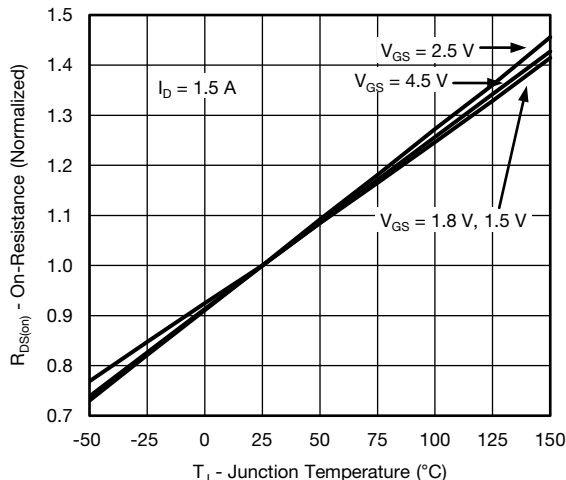


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	17	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-2.6	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.4	-	0.85	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = 4.5 V	10	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 1.5 A	-	0.030	0.037	Ω
		V _{GS} = 2.5 V, I _D = 1 A	-	0.033	0.041	
		V _{GS} = 1.8 V, I _D = 1 A	-	0.038	0.047	
		V _{GS} = 1.5 V, I _D = 0.5 A	-	0.044	0.068	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1.5 A	-	17	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	620	-	pF
Output Capacitance	C _{oss}		-	110	-	
Reverse Transfer Capacitance	C _{rss}		-	40	-	
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 8 V, I _D = 1.5 A	-	10.4	16	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 1.5 A	-	5.9	9	
			-	0.7	-	
			-	0.66	-	
Gate-Source Charge	Q _{gs}					
Gate-Drain Charge	Q _{gd}					
Gate Resistance	R _g	V _{GS} = 0.1 V, f = 1 MHz	-	5.3	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 6.7 Ω I _D ≅ 1.5 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	5	10	ns
Rise Time	t _r		-	25	50	
Turn-Off Delay Time	t _{d(off)}		-	26	50	
Fall Time	t _f		-	10	20	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 6.7 Ω I _D ≅ -1.5 A, V _{GEN} = -8 V, R _g = 1 Ω	-	5	10	
Rise Time	t _r		-	22	45	
Turn-Off Delay Time	t _{d(off)}		-	23	45	
Fall Time	t _f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _A = 25 °C	-	-	1.5	A
Pulse Diode Forward Current	I _{SM}		-	-	20	
Body Diode Voltage	V _{SD}	I _S = 1.5 A, V _{GS} = 0	-	0.7	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1.5 A, dI/dt = 100 A/μs, T _J = 25 °C	-	15	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	6	15	nC
Reverse Recovery Fall Time	t _a		-	8.5	-	ns
Reverse Recovery Rise Time	t _b		-	6.5	-	

Notes

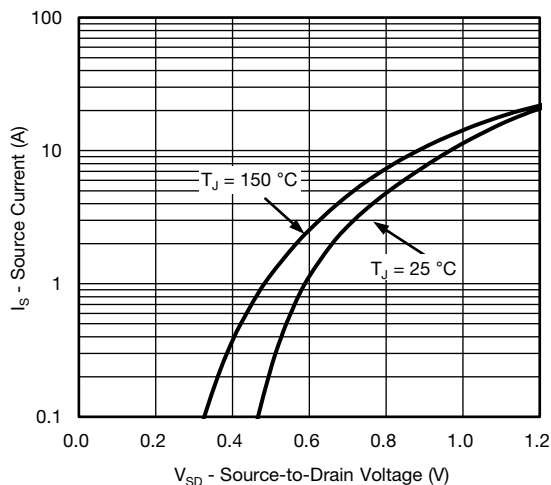
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

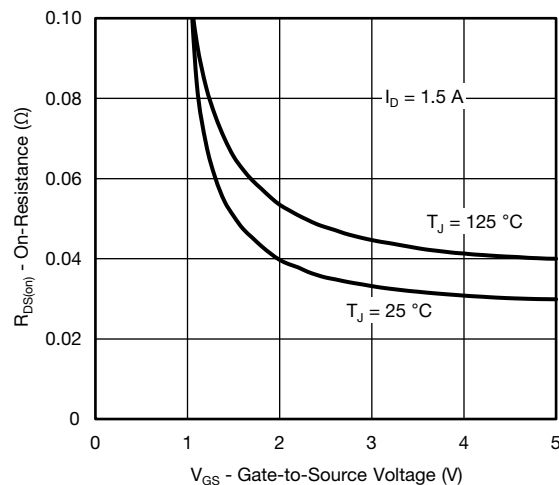
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



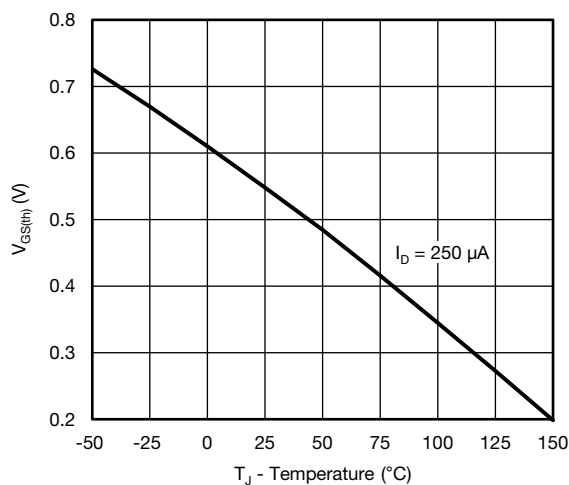
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



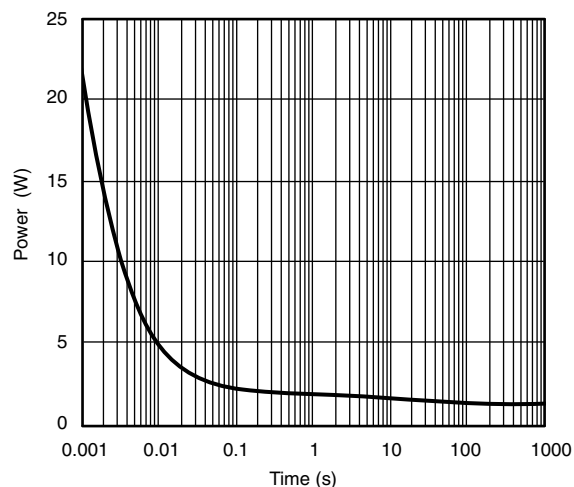
Source-Drain Diode Forward Voltage



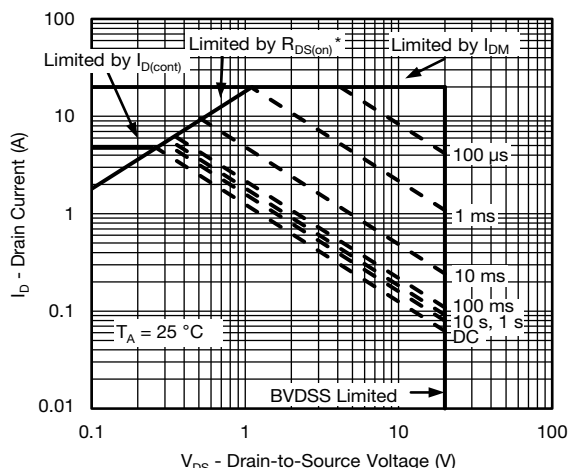
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

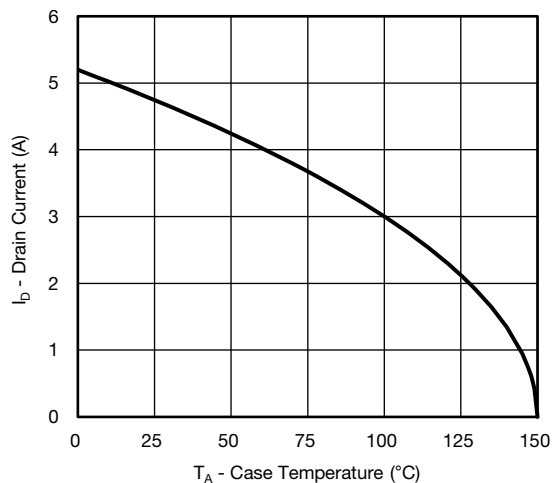
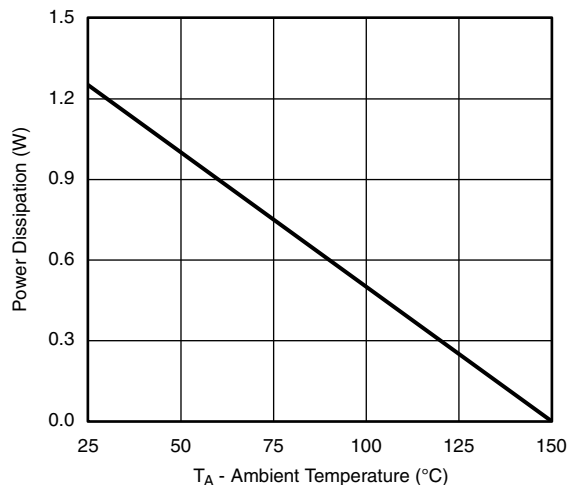


Single Pulse Power, Junction-to-Ambient



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

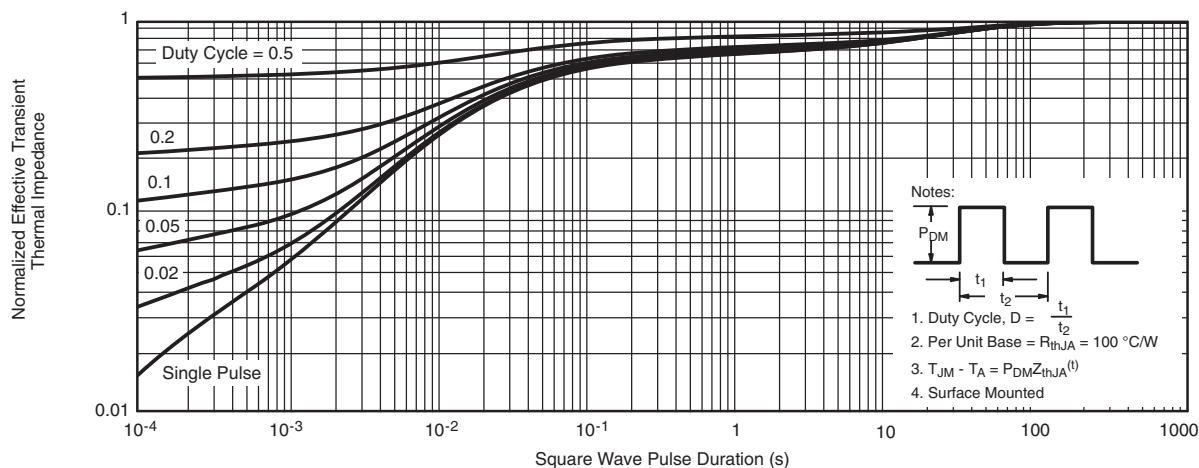
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power Derating
Note

- When mounted on 1" x 1" FR4 with full copper.

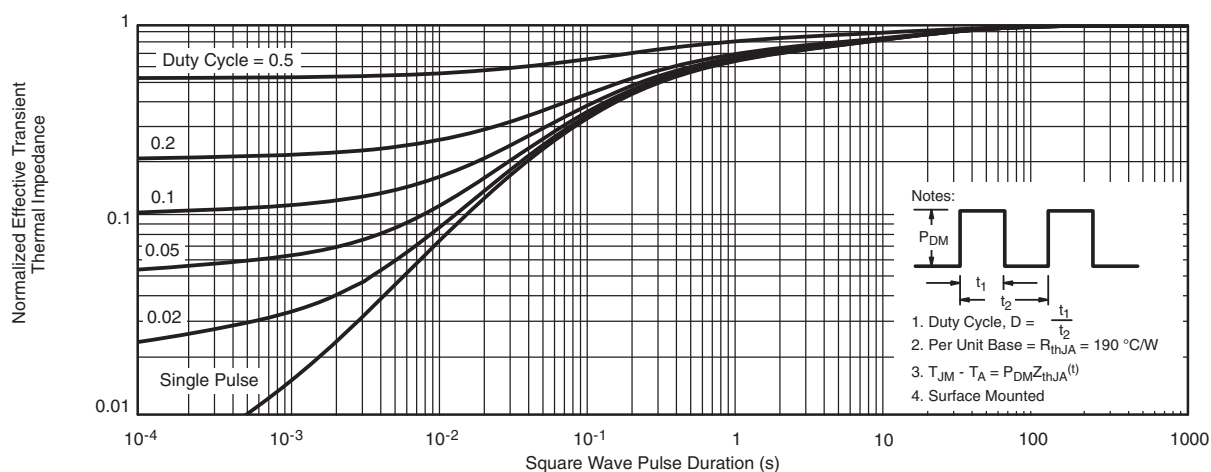
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



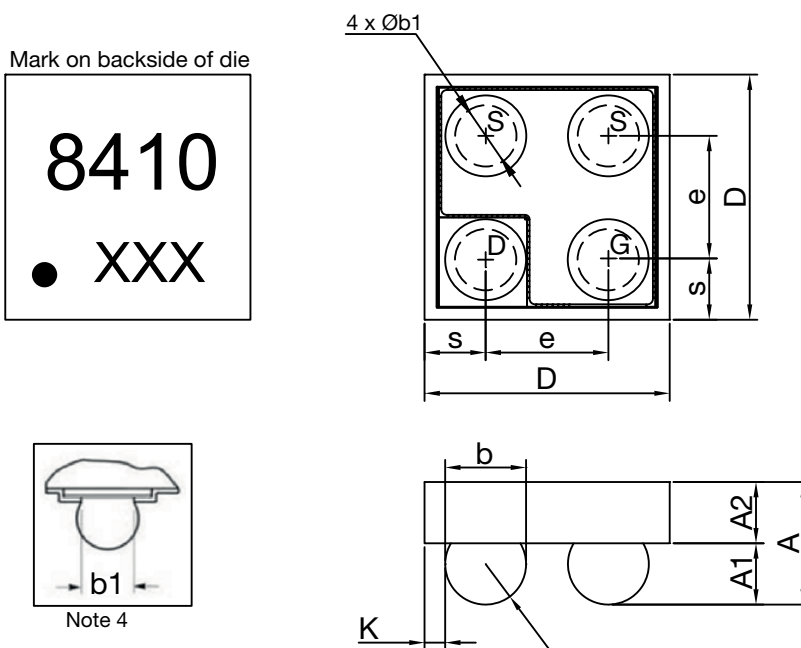
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)

PACKAGE OUTLINE
MICRO FOOT 1 mm x 1 mm: 4-Bump (0.5 mm pitch)

Notes

- (1) Laser mark on the backside surface of die.
- (2) Bumps are 95.5 % Sn, 3.8 % Ag, 0.7 % Cu.
- (3) • is location of pin 1.
- (4) “b1” is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
- (5) Non-solder mask defined copper landing pad.

DIMENSION	MILLIMETERS ^a			INCHES		
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM
A	0.460	0.500	0.540	0.0181	0.0196	0.0212
A1	0.214	0.250	0.286	0.0084	0.0098	0.0112
A2	0.244	0.254	0.264	0.0096	0.0100	0.0104
b	0.297	0.330	0.363	0.0116	0.0129	0.0142
b1		0.250			0.0098	
e		0.500			0.0197	
s	0.210	0.230	0.250	0.0008	0.0090	0.0098
D	0.920	0.960	1.000	0.0362	0.0377	0.0393
K	0.028	0.065	0.101	0.0011	0.0025	0.0039

Note

- a. Use millimeters as the primary measurement.

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