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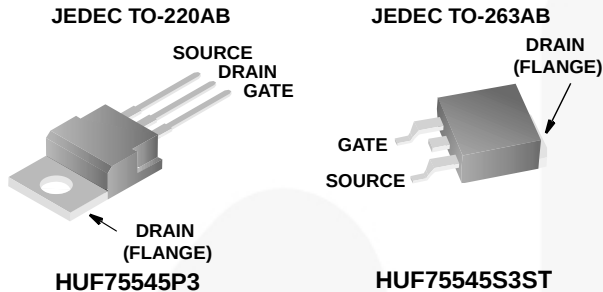
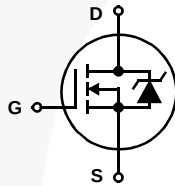


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N-Channel UltraFET Power MOSFET
80 V, 75 A, 10 mΩ
Packaging

Symbol

Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.010\Omega$, $V_{GS} = 10V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75545P3	TO-220AB	75545P
HUF75545S3ST	TO-263AB	75545S

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HUF75545P3, HUF75545S3ST	UNITS
Drain to Source Voltage (Note 1)	80	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	80	V
Gate to Source Voltage	± 20	V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	75	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	73	A
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating	Figure 6	
Power Dissipation	270	W
Derate Above 25°C	1.8	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief TB334.	260	$^\circ\text{C}$

NOTES:

1. $T_J = 25^\circ\text{C}$ to 150°C .

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

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HUF75545P3, HUF75545S3S

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	80	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 75V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 70V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figure 9)	-	0.0082	0.010	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-220 and TO-263	-	-	0.55	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 40V, I _D = 75A V _{GS} = 10V, R _{GS} = 2.5Ω	-	-	210	ns	
Turn-On Delay Time	t _{d(ON)}		-	14	-	ns	
Rise Time	t _r		-	125	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	40	-	ns	
Fall Time	t _f		-	90	-	ns	
Turn-Off Time	t _{OFF}		-	-	195	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 40V, I _D = 75A, I _{g(REF)} = 1.0mA (Figure 13)	-	195	235	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	105	125	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	6.8	8.2	nC
Gate to Source Gate Charge	Q _{gs}			-	15	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	43	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 12)	-	3750	-	pF	
Output Capacitance	C _{OSS}		-	1100	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	350	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75\text{A}$	-	-	1.25	V
		$I_{SD} = 35\text{A}$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	300	nC

Typical Performance Curves

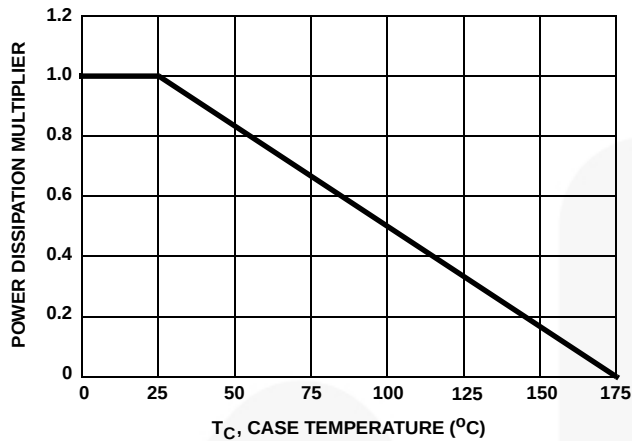


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

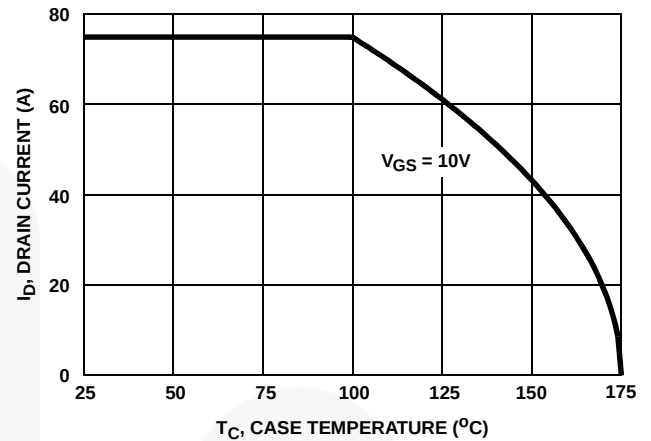


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

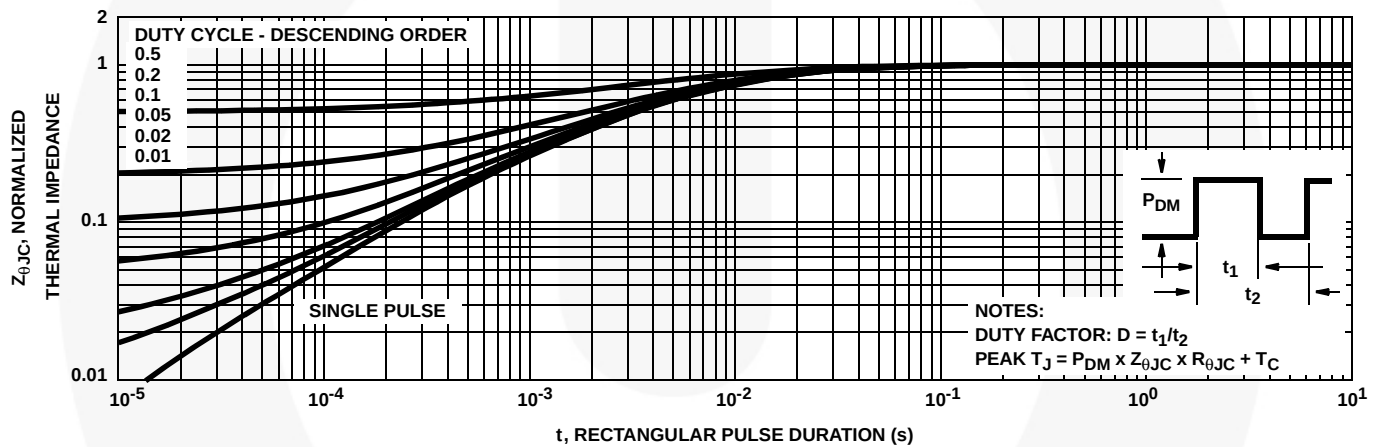


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

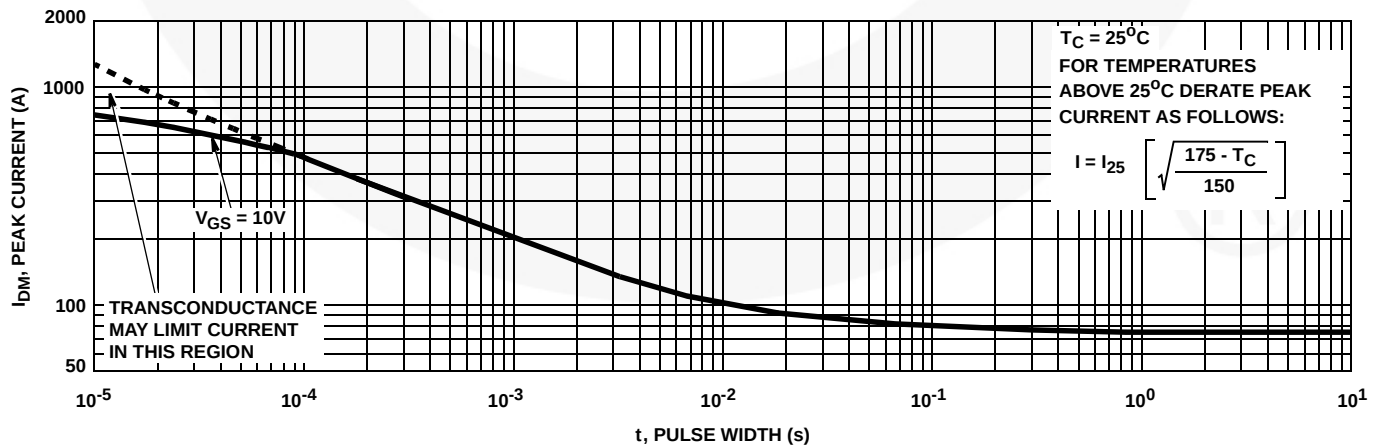


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

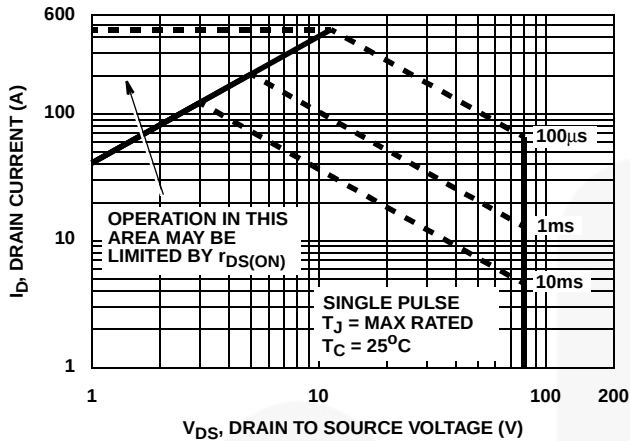
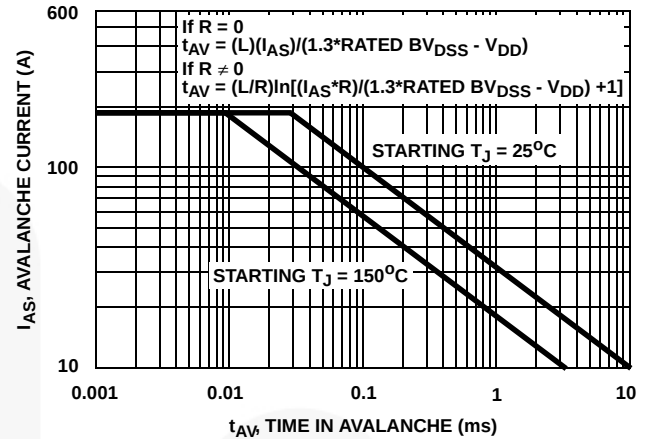


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

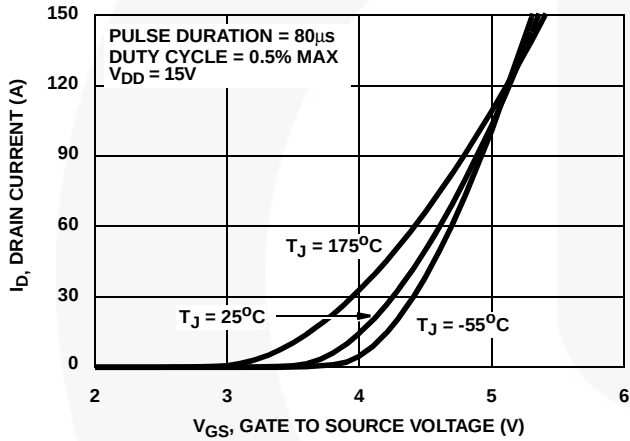


FIGURE 7. TRANSFER CHARACTERISTICS

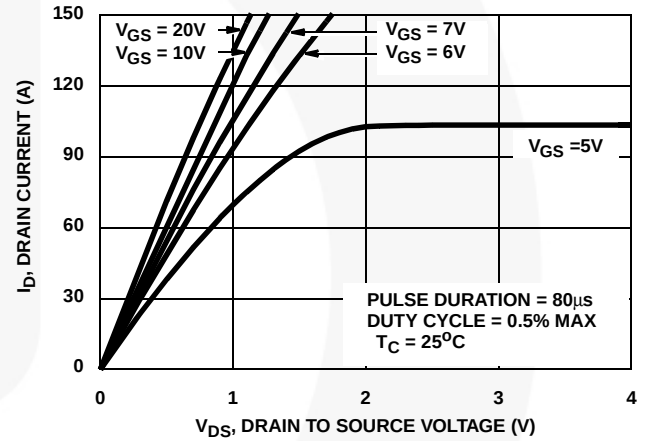


FIGURE 8. SATURATION CHARACTERISTICS

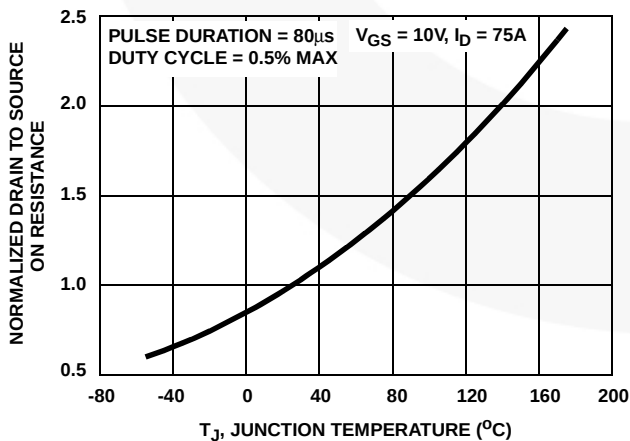


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

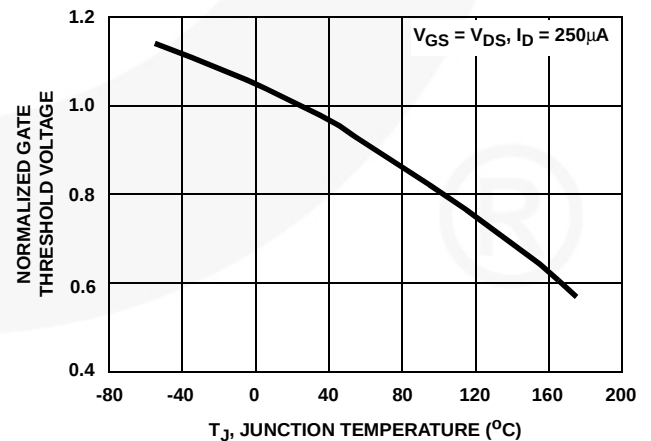


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

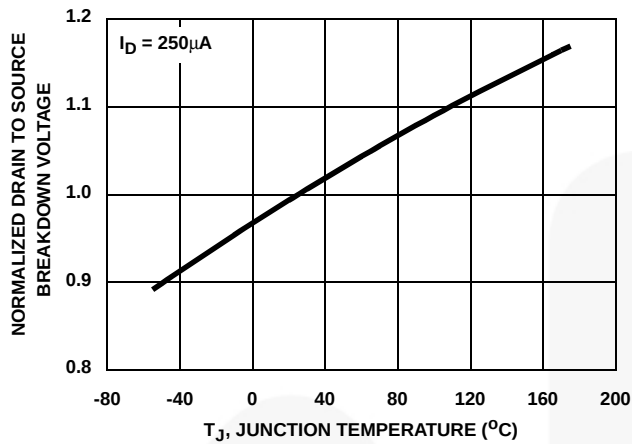


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

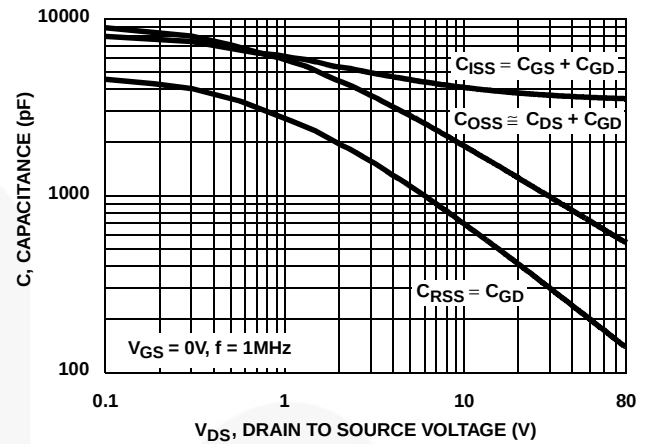
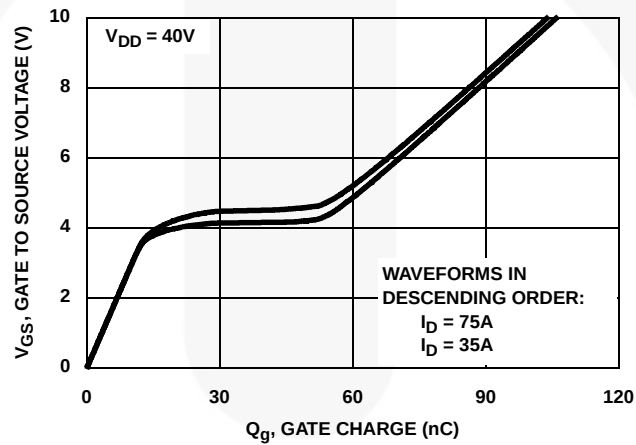


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

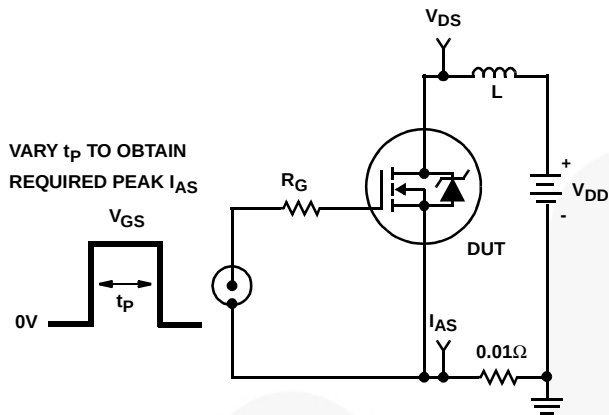


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

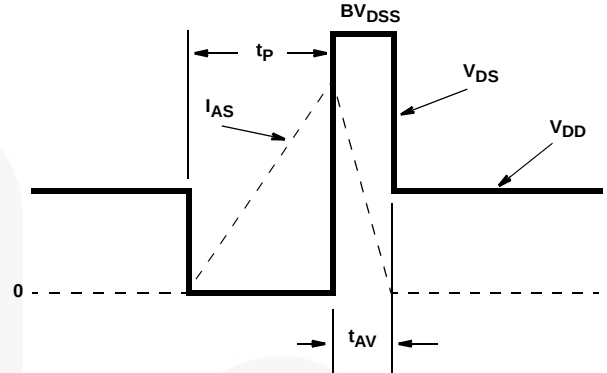


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

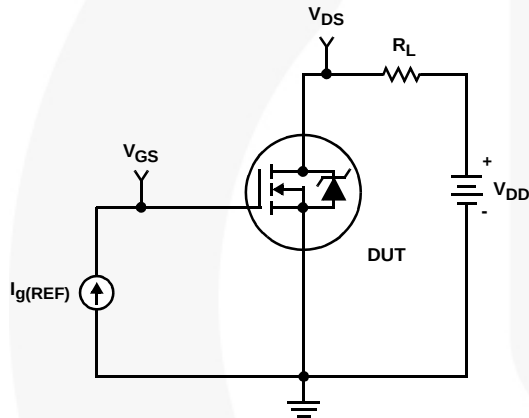


FIGURE 16. GATE CHARGE TEST CIRCUIT

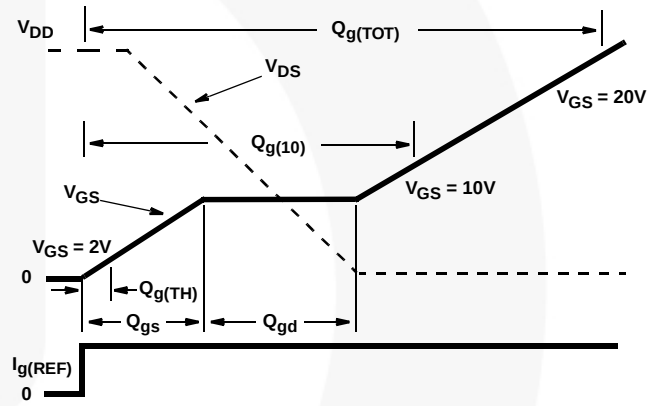


FIGURE 17. GATE CHARGE WAVEFORMS

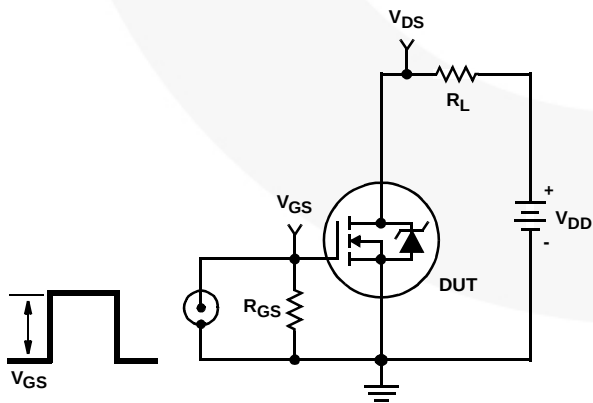


FIGURE 18. SWITCHING TIME TEST CIRCUIT

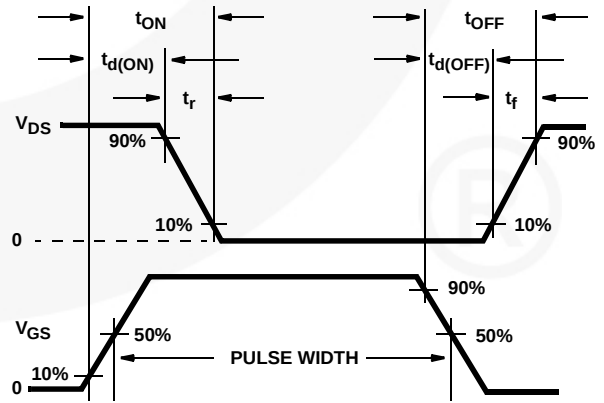


FIGURE 19. SWITCHING TIME WAVEFORM

SPICE Thermal Model

REV 21 May 1999

HUF75545T

CTHERM1 th 6 6.4e-3
 CHERM2 6 5 3.0e-2
 CHERM3 5 4 1.4e-2
 CHERM4 4 3 1.6e-2
 CHERM5 3 2 5.5e-2
 CHERM6 2 tl 1.5

RHERM1 th 6 3.2e-3
 RHERM2 6 5 8.1e-3
 RHERM3 5 4 2.3e-2
 RHERM4 4 3 1.3e-1
 RHERM5 3 2 1.8e-1
 RHERM6 2 tl 3.8e-2

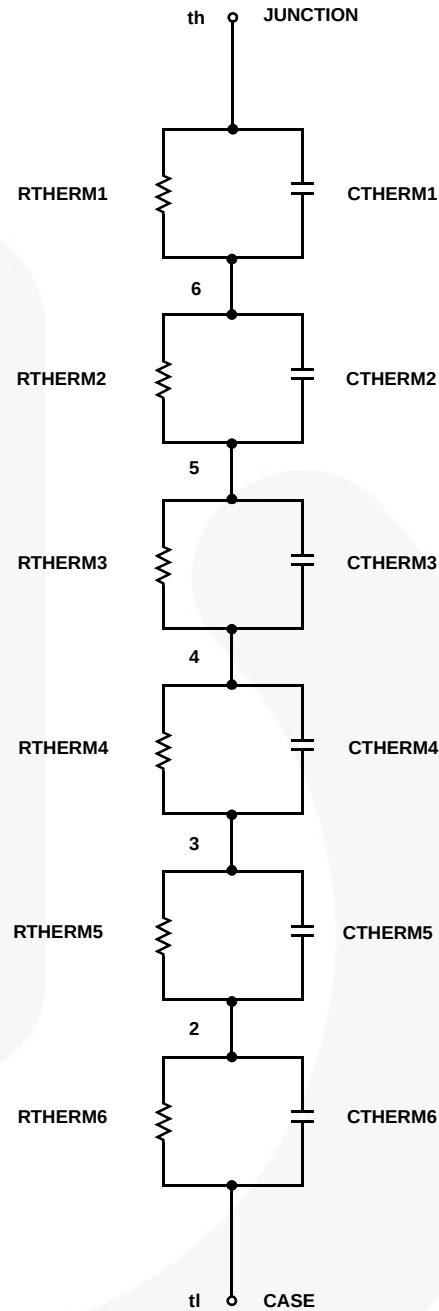
SABER Thermal Model

SABER thermal model HUF75545T

template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.therm1 th 6 = 6.4e-3
    ctherm.therm2 6 5 = 3.0e-2
    ctherm.therm3 5 4 = 1.4e-2
    ctherm.therm4 4 3 = 1.6e-2
    ctherm.therm5 3 2 = 5.5e-2
    ctherm.therm6 2 tl = 1.5
}
```

```
rtherm.rtherm1 th 6 = 3.2e-3
rtherm.rtherm2 6 5 = 8.1e-3
rtherm.rtherm3 5 4 = 2.3e-2
rtherm.rtherm4 4 3 = 1.3e-1
rtherm.rtherm5 3 2 = 1.8e-1
rtherm.rtherm6 2 tl = 3.8e-2
}
```





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