

DATA SHEET

SE5023L: 5 GHz, +26 dBm Power Amplifier with Power Detector

Applications

- DSSS 5 GHz WLAN (IEEE 802.11ac)
- DSSS 5 GHz WLAN (IEEE 802.11n)
- Access points, PCMCIA, PC cards

Features

- 5 GHz matched +24 dBm 802.11ac power amplifier
- External analog reference voltage (VREF) for maximum flexibility
- Buffered, temperature compensated power detector
- 1.8% EVM, +24 dBm, 256 QAM, 802.11ac
3% EVM, +26 dBm, 64 QAM, 802.11n
- 32 dB Gain
- Lead-free, RoHS-compliant and halogen-free
(20-pin, 4 × 4 × 0.9 mm) QFN package (MSL1, 260 °C per JEDEC J-STD-020)

Description

The SE5023L is a 5 GHz power amplifier offering high linear power for wireless LAN applications.

The SE5023L offers a high level of integration for a simplified design, providing quicker time to market and higher application board production yield. The device integrates all matching elements, a temperature compensated, load insensitive power detector with 15 dB of dynamic range and a 3.8 GHz notch filter.

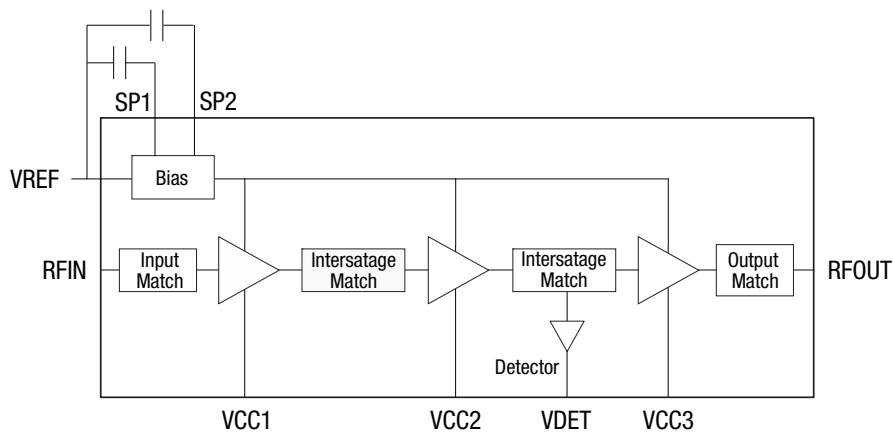
For wireless LAN applications, the device meets the requirements of IEEE 802.11ac and 802.11n, and delivers approximately +24 dBm of 802.11ac output power or +26 dBm of 802.11n output power at 5 V.

A 2.85 V reference voltage on VREF is all that is required to enable or disable the power amplifier.

A block diagram of the SE5023L is shown in Figure 1. The device pinout for the 20-pin QFN are shown in Figure 2. Signal pin assignments and functional pin descriptions are described in Table 1.



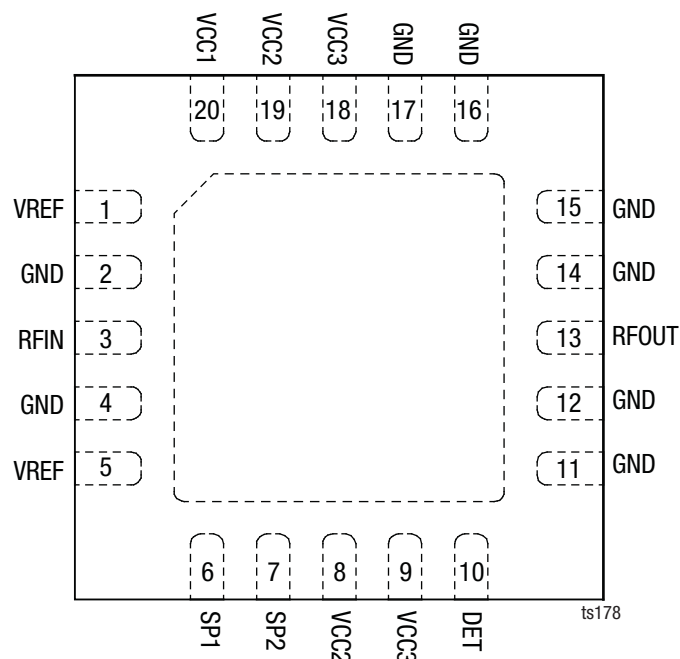
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Note: RFIN and RFOUT include DC shunt to Ground.
External blocking capacitors are recommended.

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Figure 1. SE5023L Block Diagram



**Figure 2. SE5023L Pinout – 20-Pin QFN
(Top View)**

Table 1. SE5023L Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	VREF	Reference voltage	9	VCC3	Third stage supply voltage
2	GND	Ground	10	DET	Analog power detector output
3	RFIN	Power amplifier RF input, DC block required	11, 12	GND	Ground
4	GND	Ground	13	RFOUT	Power amplifier RF output
5	VREF	Reference voltage	14, 15, 16, 17	GND	Ground
6	SP1	Port for optional capacitor to improve dynamic EVM	18	VCC3	Third stage supply voltage
7	SP2	Port for optional capacitor to improve dynamic EVM	19	VCC2	Second stage supply voltage
8	VCC2	Second stage supply voltage	20	VCC1	First stage supply voltage

Electrical and Mechanical Specifications

The absolute maximum ratings of the SE5023L are provided in Table 2. Recommended operating conditions are specified in

Table 3. Electrical specifications are provided in Tables 4 through 6. Figure 3 shows the power detector characteristics.

Table 2. SE5023L Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage on pins VCC3	VCC	−0.3	+6	V
Supply voltage on pins VCC1, VCC2		−0.3	VCC3	V
Power amplifier enable and reference voltage	VREF	−0.3	+3.6	V
RF input power, RFOUT into 50 Ω match, TCASE_MAX = 85 °C	RFIN		+6	dBm
Storage temperature range	TSTG	−40	+160	°C
Maximum junction temperature	TJ		+160	°C
Electrostatic discharge: Human Body Model (HBM), Class 1B	ESD		500	V

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. SE5023L Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage VCC3	VCC	3.0	5.5	V
Supply voltage VCC1, VCC2		3.0	VCC3	V
Maximum case temperature	TCASE_MAX	−40	+85	°C
Reference voltage	VREF	2.8	2.9	V

Table 4. SE5023L Electrical Specifications: DC Characteristics (Note 1)

(VCC = 5.0 V, VREF = 2.85 V, TA = +25 °C as Measured on Skyworks' SE5023L-EK1 Evaluation Board, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply current	ICC_802.11a	POUT = 26 dBm, 54 Mbps, 64 QAM,			600	mA
Quiescent current	IQC	No RF	150		300	mA
Supply current	IOFF	VREF = 0 V, no RF		0.5	10	μ A
Bias control current	IEN	VREF = VREF_H, Internal 2 k Ω pull down resistor		10		mA
Reference voltage enabled	VREF_H		2.80	2.85	2.9	V
Reference voltage current	IREF	VREF voltage set to 2.85 V		10		mA
Reference voltage disabled	VREF_L		0		0.5	V

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 5. SE5023L Electrical Specifications: AC Characteristics (Note 1)**(V_{CC} = 5.0 V, V_{REF} = 2.85 V, f = 5.4 GHz, T_A = +25 °C as Measured on the SE5023L-EK1 Evaluation Board, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f _L _U		5.15		5.85	GHz
Output power	P _{OUT}	MCS9, –35 dB DEVM, UNII-1 UNII-2 & 3	+17 +22	+19 +24		dBm dBm
		MCS9, –30 dB DEVM UNII-1 UNII-2 & 3	+22 +24	+24 +26		dBm dBm
		MCS0, mask limited UNII-1 UNII-2 & 3	+25 +27	+27 +29		dBm dBm
Output 1 dB compression point	P _{1dB}	No modulation		+34		dBm
Small signal gain	S ₂₁	P _{IN} = –25 dBm	28	32	34	dB
Small signal gain variation	ΔS ₂₁	Within each UNII Band		3		dB
Gain at 3.8 GHz	S _{21_3.8}	P _{IN} = –25 dBm			0	dB
Harmonic	2f	P _{OUT} = +26 dBm, 5 V			–45	dBm/MHz
	3f					
Rise and fall time	t _r , t _f			0.15	0.3	μs
Stability	STAB	P _{OUT} = +26 dBm, V _{CC} = 5 V, 54 Mbps, 64QAM, VSWR = 6:1, all phases	All non-harmonically related outputs less than –50 dBc/100 kHz			
Tolerance to constant input power into a mismatch load	Ruggedness	P _{IN} = –10 dBm, CW, VSWR = 6:1, all phases	No damage			

Note 1: Performance is guaranteed only under the conditions listed in this table.**Table 6. SE5023L Electrical Specifications: Power Detector Characteristics (Note 1)****(V_{CC} = 5.0 V, V_{REF} = 2.85 V, f = 5.4 GHz, T_A = +25 °C as Measured on the SE5023L-EK1 Evaluation Board, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
P _{OUT} detect range	P _{DR}		0		P _{1dB}	dBm
Detector voltage	V _{DET}	P _{OUT} = +26 dBm	0.8		1.2	V
		P _{OUT} = No RF	0.22		0.33	V
Detector accuracy	ERR _{DET}	ΔP _{OUT} at constant V _{DET} , 5.15 GHz to 5.70 GHz	–0.5		+0.5	dB
		5.70 GHz to 5.85 GHz	–0.5		+0.5	dB
		ΔP _{OUT} at constant V _{DET} , VSWR = 3:1	–1.5		+1.5	dB
Output impedance	PDZ _{OUT}			0.7		kΩ
DC load impedance	PDZ _{LOAD}			26.5		kΩ

Note 1: Performance is guaranteed only under the conditions listed in this table.

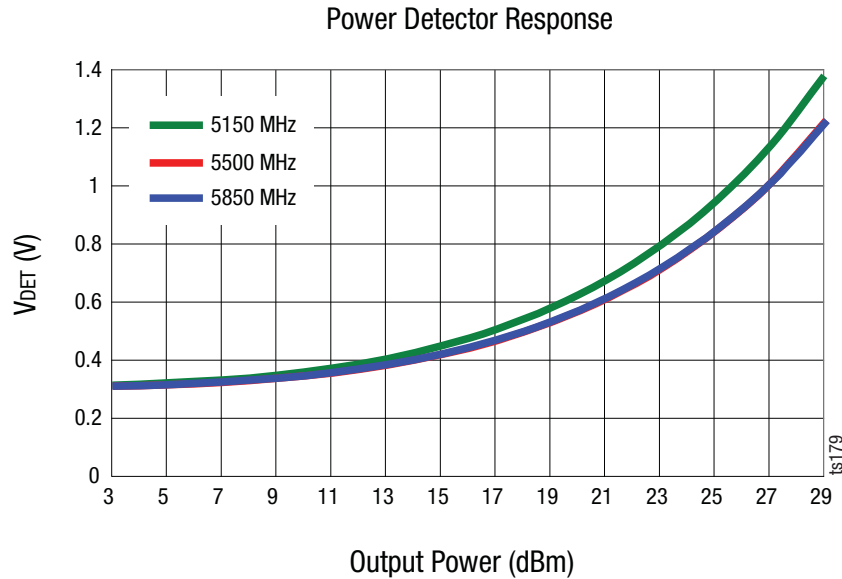


Figure 3. SE5023L Power Detector Characteristic over Frequency

Package Dimensions

The PCB layout footprint for the SE5023L is provided in Figure 4. Typical part markings are shown in Figure 5. Package dimensions for the 20-pin QFN are shown in Figure 6, and carrier tape dimensions are provided in Figure 7.

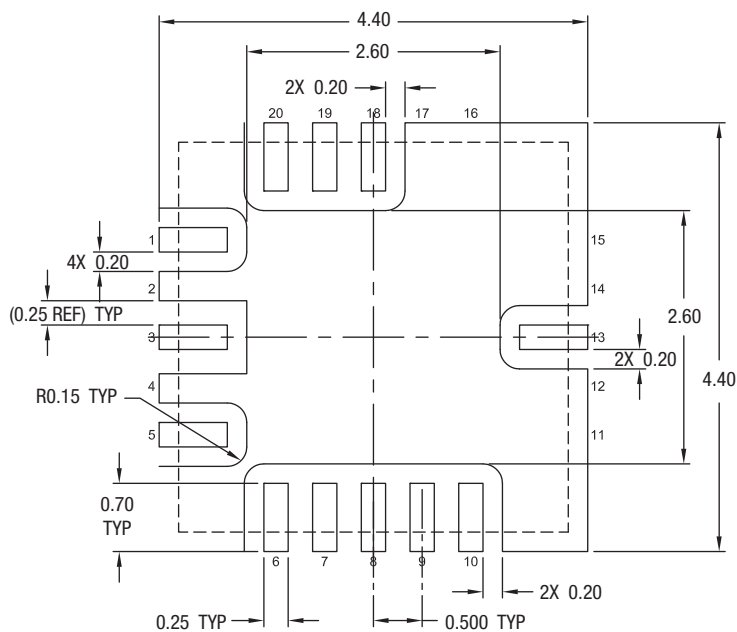
Package Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur

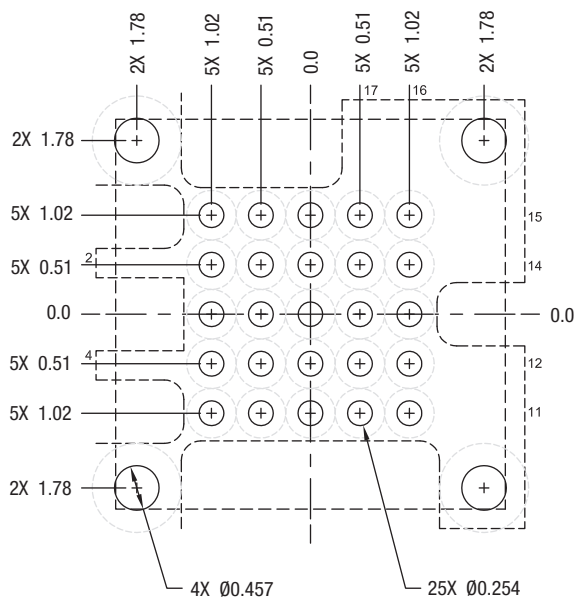
when the part is subjected to high temperature during solder assembly.

The SE5023L is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

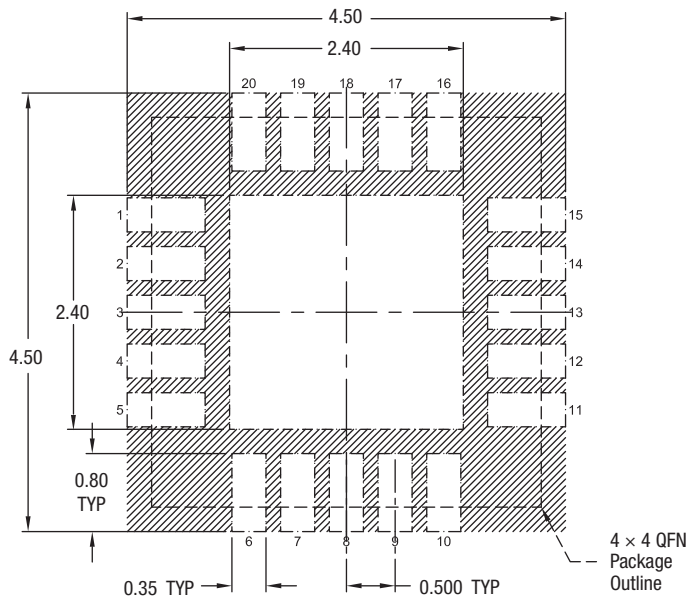
Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



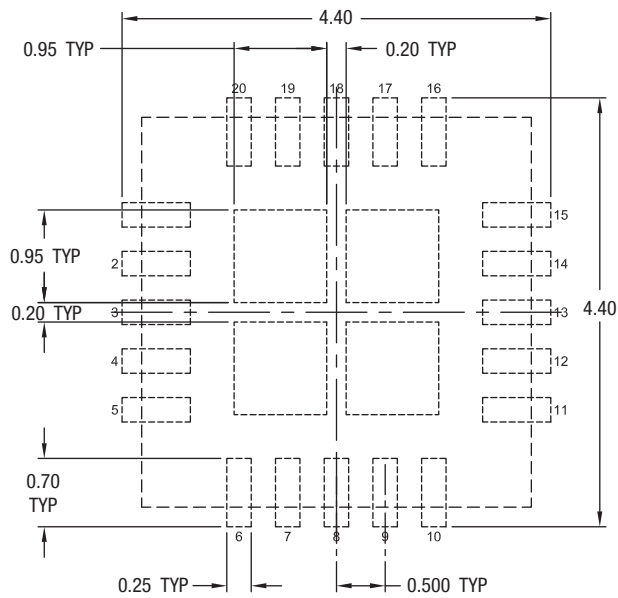
Board Metal



Via Pattern (Note 4)



Solder Mask Pattern (Note 6)



Stencil Pattern (Note 5)
(61% solder coverage on center Pad)

Notes:

1. All dimensions are in millimeters.
2. Interpret dimensioning and tolerancing per ASME Y14.5M-1994.
3. Unless specified, dimensions are symmetrical about center lines.
4. Via hole recommendations: 0.025 mm Cu via wall plating (minimum). Via holes to be filled with conductive paste and plated over.
5. Stencil recommendations: 0.125 mm stencil thickness, laser cut apertures, trapezoidal walls and rounded corners will offer better paste release.
6. Solder mask recommendations: contact board fabricator for recommended solder mask offset and tolerance.

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Figure 4. PCB Layout Footprint for the SE5023L

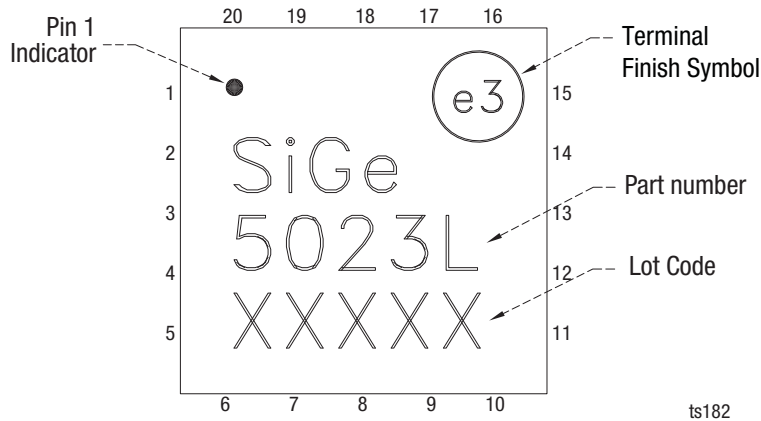
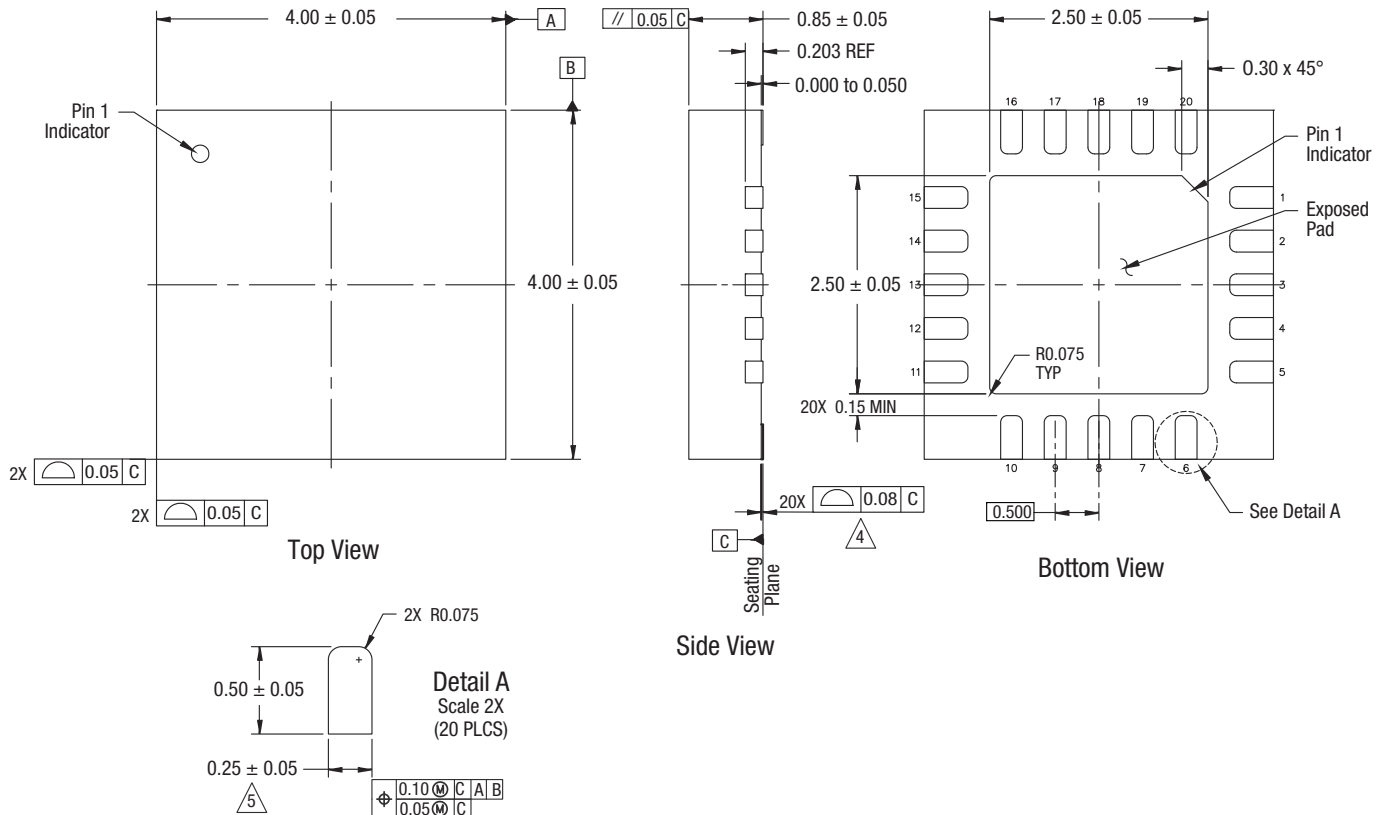


Figure 5. Typical Part Markings (Top View)

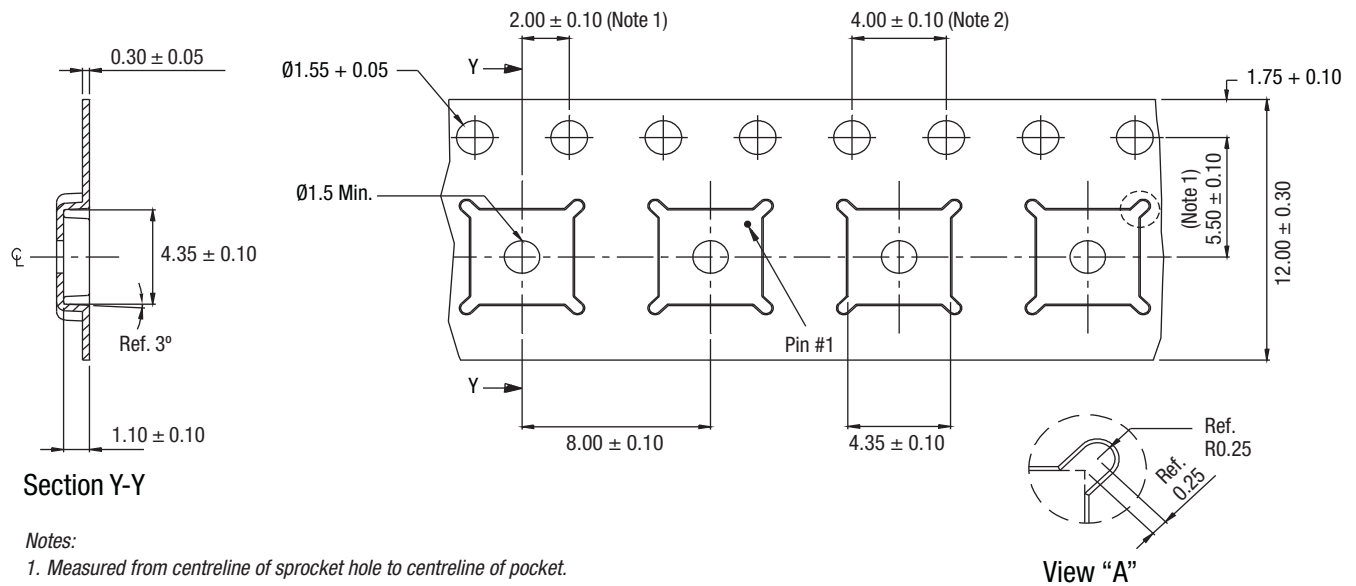


Notes:

1. All measurements are in millimeters.
2. Dimensioning and tolerancing according to ASME Y14.5M-1994.
3. Tolerancing (unless otherwise specified):
 Decimal Tolerance: X.X (1 PLC) ± 0.1 mm
 X.XX (2 PLCs) ± 0.05 mm
 X.XXX (3 PLCs) ± 0.025 mm
 Angular Tolerance: $\pm 1^\circ/2^\circ$
4. Coplanarity applies to the exposed center ground pad as well as the terminal.
5. Dimension applies to metalized terminal. If the terminal has a radius, the dimension should not be measured in the radius area.
6. Plating requirements per source control drawing (SCD) 2504.
7. Unless specified, dimensions are symmetrical about center lines.

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Figure 6. SE5023L 20-Pin QFN Package Dimensions



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Figure 7. SE5023L 20-pin QFN Carrier Tape Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SE5023L: 5 GHz, 26 dBm Power Amplifier with Power Detector	SE5023L	SE5023L-EK1

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