

1:4 Differential LVDS Fanout Buffer with Selectable Clock Input

Features

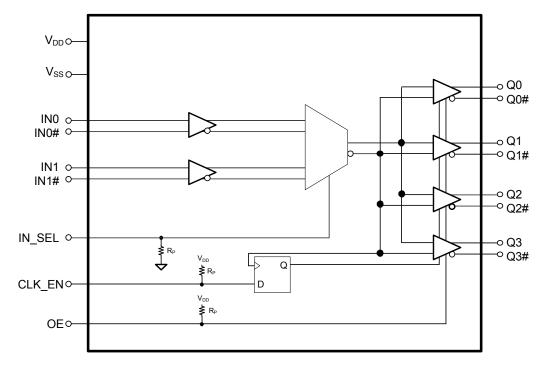
- Select one of two differential (LVPECL, LVDS, HCSL, or CML) input pairs to distribute to four LVDS output pairs
- Translates any single-ended input signal to 3.3 V LVDS levels with resistor bias on INx# input
- 30 ps maximum output-to-output skew
- 480 ps maximum propagation delay
- 0.11 ps maximum additive RMS phase jitter at 156.25 MHz (12 kHz to 20 MHz offset)
- Up to 1.5 GHz operation
- Output enable and synchronous clock enable functions
- 20-pin TSSOP
- 2.5 V or 3.3 V operating voltage [1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DL1504 is an ultra-low noise, low-skew, low-propagation delay 1:4 differential LVDS fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DL1504 can select between two separate differential (LVPECL, LVDS, HCSL, or CML) input clock pairs using the IN_SEL pin. The synchronous clock enable function ensures glitch-free output transitions during enable and disable periods. The output enable function allows the outputs to be asynchronously driven to a high-impedance state. The device has a fully differential internal architecture that is optimized to achieve low-additive jitter and low-skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, click here.

Logic Block Diagram



Note

^{1.} Input AC-coupling capacitors are required for voltage-translation applications.



Contents

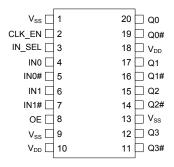
Pinouts	3
Pin Definitions	3
Absolute Maximum Ratings	4
Operating Conditions	
DC Electrical Specifications	
Thermal Resistance	
AC Electrical Specifications	
Switching Waveforms	
Application Information	
Ordering Information	
Ordering Code Definitions	

Package Diagram	12
Acronyms	13
Document Conventions	13
Units of Measure	13
Document History Page	14
Sales, Solutions, and Legal Information	16
Worldwide Sales and Design Support	16
Products	16
PSoC®Solutions	16
Cypress Developer Community	16
Technical Support	16



Pinouts

Figure 1. 20-pin TSSOP pinout



Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1, 9, 13	V _{SS}	Power	Ground
2	CLK_EN	Input	Synchronous clock enable. LVCMOS/LVTTL; When CLK_EN = Low, Q(0:3) outputs are held low and Q(0:3)# outputs are held high
3	IN_SEL	Input	Input clock select pin. LVCMOS/LVTTL; When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
4	IN0	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = Low
5	IN0#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = Low
6	IN1	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = High
7	IN1#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = High
8	OE	Input	Output enable. LVCMOS/LVTTL; When OE = Low, Q(0:3) and Q(0:3)# outputs are disabled (see I _{OZ})
10, 18	V_{DD}	Power	Power supply
11, 14, 16, 19	Q(0:3)#	Output	LVDS complementary output clocks
12, 15, 17, 20	Q(0:3)	Output	LVDS output clocks



Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Nonfunctional	-0.5	4.6	V
V _{IN} ^[2]	Input voltage, relative to V _{SS}	Nonfunctional	-0.5	Lesser of 4.0 or V _{DD} + 0.4	V
V _{OUT} ^[2]	DC output or I/O voltage, relative to V _{SS}	Nonfunctional	-0.5	Lesser of 4.0 or V _{DD} + 0.4	V
T_S	Storage temperature	Nonfunctional	– 55	150	°C
ESD _{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	_	V
L _U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		D78B
UL-94	Flammability rating	At 1/8 in.	V-0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5 V supply	2.375	2.625	V
		3.3 V supply	3.135	3.465	V
T _A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	-40	85	°C
t _{PU}	Power ramp time	Power-up time for V _{DD} to reach minimum specified voltage. (Power ramp must be monotonic)	0.05	500	ms

Document Number: 001-56312 Rev. *L

Note
2. The voltage on any I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.



DC Electrical Specifications

(V_{DD} = 3.3 V \pm 5% or 2.5 V \pm 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I _{DD}	Operating supply current	All LVDS outputs terminated with a load of 100 $\Omega^{[3,4]}$	-	61	mA
V _{IH1}	Input high voltage, differential input clocks, IN0, IN0#, IN1, and IN1#		_	V _{DD} + 0.3	V
V _{IL1}	Input low voltage, differential input clocks, IN0, IN0#, IN1, and IN1#		-0.3	_	V
V _{IH2}	Input high voltage, CLK_EN, IN_SEL, and OE	V _{DD} = 3.3 V	2.0	V _{DD} + 0.3	V
V _{IL2}	Input low voltage, CLK_EN, IN_SEL, and OE	V _{DD} = 3.3 V	-0.3	0.8	V
V _{IH3}	Input high voltage, CLK_EN, IN_SEL, and OE	V _{DD} = 2.5 V	1.7	V _{DD} + 0.3	V
V _{IL3}	Input low voltage, CLK_EN, IN_SEL, and OE	V _{DD} = 2.5 V	-0.3	0.7	V
V _{ID_LVDS} ^[5]	LVDS input differential amplitude	See Figure 3 on page 8	0.4	0.8	V
V _{ID_LVPECL} ^[5]	LVPECL/CML/HCSL input differential amplitude	See Figure 3 on page 8	0.4	1.0	V
V _{ICM}	Input common mode voltage	See Figure 3 on page 8	0.2	V _{DD} – 0.2	V
I _{IH}	Input high current, All inputs	Input = V _{DD} ^[6]	-	150	μΑ
I _{IL}	Input low current, All inputs	Input = V _{SS} ^[6]	-150	-	μΑ
V _{PP}	LVDS differential output voltage peak to Peak, Single-ended	V_{DD} = 3.3 V or 2.5 V, R _{TERM} = 100 Ω between Q and Q# pairs [3, 7]	250	470	mV
V _{OCM}	LVDS differential output common mode voltage	V_{DD} = 3.3 V or 2.5 V, R _{TERM} = 100 Ω between Q and Q# pairs [3, 7]	1.125	1.375	V
ΔV_{OCM}	Change in V _{OCM} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs ^[3, 7]	-	50	mV
I _{OZ}	Output leakage current	OE = V _{SS} , V _{OUT} = 0.75 V–1.75 V	– 15	15	μΑ
R _P	Internal pull-up/pull-down resistance, LVCMOS logic inputs	CLK_EN has pull-up only IN_SEL has pull-down only OE has pull-up only	60	165	kΩ
C _{IN}	Input capacitance	Measured at 10 MHz; per pin	-	3	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	20-pin TSSOP	Unit
- 3/1	(junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in		°C/W
θ_{JC}	Thermal resistance (junction to case)	accordance with EIA/JESD51.	16	°C/W

Notes

- Notes

 Refer to Figure 2 on page 8.

 IDD includes current that is dissipated externally in the output termination resistors.

 VID minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with VID minimum of greater than 200 mV.

 Positive current flows into the input pin, negative current flows out of the input pin.

 Refer to Figure 4 on page 8.

 These parameters are guaranteed by design and are not tested.

Document Number: 001-56312 Rev. *L



AC Electrical Specifications

(V_{DD} = 3.3 V \pm 5% or 2.5 V \pm 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Тур	Max	Unit
F _{IN}	Input frequency	Differential Input	DC	_	1.5	GHz
		Single ended input [9]	DC	_	250	MHz
F _{OUT}	Output frequency	F _{OUT} = F _{IN,} Differential Input	DC	_	1.5	GHz
		F _{OUT} = F _{IN,} Single ended input ^[9]	DC	_	250	MHz
t _{PD} ^[10]	Propagation delay differential input pair to differential output pair	Input rise/fall time < 1.5 ns (20% to 80%)	-	_	480	ps
t _{ODC} ^[11]	Output duty cycle	Diff input at 50% duty cycle Frequency range up to 1 GHz	48	-	52	%
		50% duty cycle at input, Frequency range up to 250MHz, Single ended input ^[9]	45	_	55	%
t _{SK1} ^[12]	Output-to-output skew	Any output to any output, with same load conditions at DUT	-	-	30	ps
t _{SK1 D} ^[12]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	-	_	150	ps
PN _{ADD}	Additive RMS phase noise 156.25 MHz Input	Offset = 1 kHz	-	-	-120	dBc/ Hz
	Rise/fall time < 150 ps (20% to 80%) V _{ID} > 400 mV or	Offset = 10 kHz	-	-	-135	dBc/ Hz
	$V_{1D} > 400 \text{ mV} \text{ or}$ Input Swing = 3.0 $V^{[9]}$	Offset = 100 kHz	-	-	-135	dBc/ Hz
		Offset = 1 MHz	-	-	-150	dBc/ Hz
		Offset = 10 MHz	-	_	-154	dBc/ Hz
		Offset = 20 MHz	-	_	–155	dBc/ Hz

^{9.} Refer to Application Information on page 10.
10. Refer to Figure 5 on page 8.
11. Refer to Figure 6 on page 8.
12. Refer to Figure 7 on page 9.



AC Electrical Specifications (continued)

(V_{DD} = 3.3 V \pm 5% or 2.5 V \pm 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Тур	Max	Unit
t _{JIT} [13]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), V _{ID} > 400 mV	_	-	0.11	ps
		156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V [14]	_	-	0.11	ps
t _R , t _F ^[15]	Output rise/fall time, single-ended	50% duty cycle at input, 20% to 80% of full swing (V _{OL} to V _{OH}) Input rise/fall time < 1.5 ns (20% to 80%) Measured at 1 GHz.	-	-	300	ps
t _{SOD}	Time from clock edge to outputs disabled	Synchronous clock enable (CLK_EN) switched low	-	-	700	ps
t _{SOE}	Time from clock edge to outputs enabled	Synchronous clock enable (CLK_EN) switched high	_	-	700	ps

Notes
13. Refer to Figure 8 on page 9.
14. Refer to Application Information on page 10.
15. Refer to Figure 9 on page 9.



Switching Waveforms

Figure 2. LVDS Output Termination

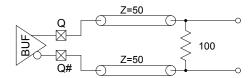


Figure 3. Input Differential and Common Mode Voltages

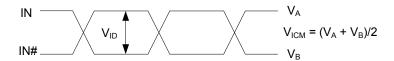


Figure 4. Output Differential and Common Mode Voltages

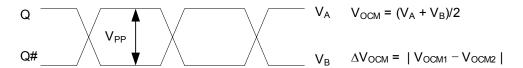


Figure 5. Input to Any Output Pair Propagation Delay

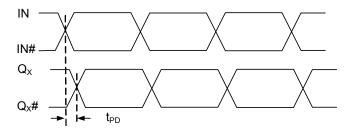
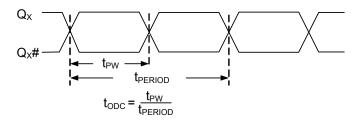


Figure 6. Output Duty Cycle





Switching Waveforms (continued)

Figure 7. Output-to-output and Device-to-device Skew

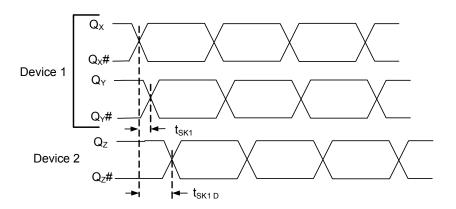
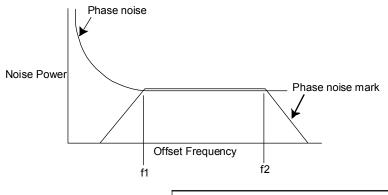
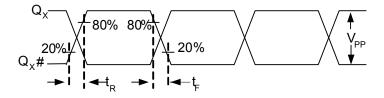


Figure 8. RMS Phase Jitter



 $RMS\ Jitter\ \infty\ \sqrt{\ Area\ Under\ the\ Masked\ Phase\ Noise\ Plot}$

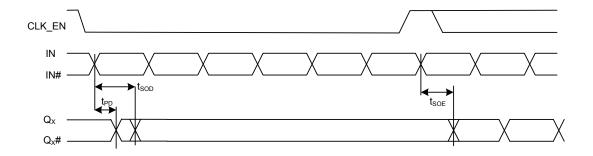
Figure 9. Output Rise/Fall Time





Switching Waveforms (continued)

Figure 10. Synchronous Clock Enable Timing



Application Information

CY2DL1504 can be used with a single ended CMOS input by biasing the Complementary Input Clock (INx#). "True" input pins (INx) of differential input pair can be fed with a single ended CMOS input signal. The "complementary" input pin (INx#) of the same differential input pair can be biased with Vref.

Figure 11 shows the schematic which can be used to give single ended CMOS input to the CY2DL1504.

The reference voltage Vref = VDD/2 is generated by the bias resistors R1, R2 and capacitor C0. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the Vref in the center of the input voltage swing. For example, if the input clock swing is 2.5 V and VDD = 3.3 V, Vref should be 1.25 V and R2/R1 = 0.609.

R2

1K

INx#

Vref

C0

0.1 u

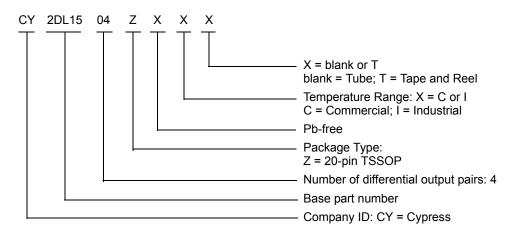
Figure 11. Single ended CMOS input given to the CY2DL1504



Ordering Information

Part Number	Туре	Production Flow
Pb-free		
CY2DL1504ZXC	20-pin TSSOP	Commercial, 0 °C to 70 °C
CY2DL1504ZXCT	20-pin TSSOP Commercial, 0 °C to 70 °C	
CY2DL1504ZXI	20-pin TSSOP Industrial, –40 °C to 85 °C	
CY2DL1504ZXIT	20-pin TSSOP Industrial, –40 °C to 85 °C	

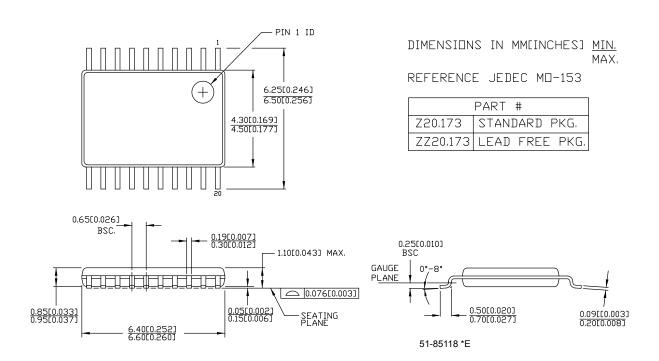
Ordering Code Definitions





Package Diagram

Figure 12. 20-pin TSSOP (4.40 mm Body) Z20.173/ZZ20.173 Package Outline, 51-85118





Acronyms

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
HCSL	high-speed current steering logic
JEDEC	joint electron devices engineering council
LVDS	low-voltage differential signal
LVCMOS	low-voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTL	low-voltage transistor-transistor logic
OE	output enable
RMS	root mean square
TSSOP	thin shrunk small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kΩ	kilohm
MHz	megahertz
μΑ	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt



Document History Page

Document Title: CY2DL1504, 1:4 Differential LVDS Fanout Buffer with Selectable Clock Input Document Number: 001-56312							
Revision	ECN	Orig. of Change	Submission Date	Description of Change			
**	2782891	CXQ	10/09/09	New data sheet.			
*A	2838613	CXQ	01/05/2010	Changed status from Advance to Preliminary. Changed from 0.34 ps to 0.25 ps maximum additive jitter in "Features" on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Added t_{PU} spec to the Operating Conditions table on page 3. Changed max I_{DD} spec in the DC Electrical Specs table on page 4 from 60 m/s to 61 mA. Removed V_{OD} and ΔV_{OD} specs from the DC Electrical Specs table on page 4 Changed I_{OZ} in the DC Electrical Specs table on page 4 from min of -10 uA to -15 uA and from max of 10 uA to 15 uA. Added R_P spec in the DC Electrical Specs table on page 4. Min = 60 k Ω , Max = 140 k Ω . Added a measurement definition for C_{IN} in the DC Electrical Specs table on page 4. Added V_{PP} and ΔV_{PP} specs to the AC Electrical Specs table on page 5. V_{PP} min = 250 mV and max = 470 mV; ΔV_{PP} max = 50 mV. Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5. Added condition to V_{RP} and V_{RP} specs in the AC Electrical specs table on page 5. Added condition to V_{RP} and V_{RP} specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%). Changed letter case and some names of all the timing parameters in Figures 4, 5, 6, 7 and 9, to be consistent with EROS. Updated Figure 4 with definition for V_{PP} and ΔV_{PP}			
*B	3010332	CXQ	08/18/2010	Changed from 0.25 ps to 0.11 ps maximum additive jitter in "Features" on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Added "Functional equivalent to ICS8543i" to the "Features" section. Changed pin 13 in Figure 1 and Table 1 from V_{DD} to V_{SS} . Changed pin 8 description in Table 1 from "high impedance" to "disabled". Added note 6 to describe I_{IH} and I_{IL} specs. Removed reference to data distribution from "Functional Description". Changed R_P for diff inputs from 100 $k\Omega$ to 150 $k\Omega$ in the Logic Block Diagran and from 60 $k\Omega$ min / 140 $k\Omega$ max to 90 $k\Omega$ min / 210 $k\Omega$ max in the DC Electrical Specs table. Split V_{ID} into separate specs in DC Electrical Specs table: 0.4 V min and 0.8 V max for LVDS, 0.4 V min and 1.0 V max for LVPECL. Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Spectable. Added "Frequency range up to 1 GHz" condition to t_{ODC} spec. Changed t_{OD} in the AC Electrical Specs table from 3 ns max to 5 ns max. Added Acronyms and Ordering Code Definition.			



Document History Page (continued)

Document Title: CY2DL1504, 1:4 Differential LVDS Fanout Buffer with Selectable Clock Input Document Number: 001-56312						
Revision	ECN	Orig. of Change	Submission Date	Description of Change		
*C	3090644	CXQ	11/19/2010	Changed V_{IN} and V_{OUT} specs from 4.0V to "lesser of 4.0 or V_{DD} + 0.4" Removed 200mA min LU spec, replaced with "Meets or exceeds JEDEC Spe JESD78B IC Latchup Test" Added " V_{OUT} = 0.75V - 1.75V" to I_{OZ} comments. Moved V_{PP} from AC spec table to DC spec table, removed ΔV_{PP} Removed R_P spec for differential input clock pins IN_X and IN_X #. Changed C_{IN} condition to "Measured at 10 MHz". Changed PN_{ADD} specs for 10kHz, 10MHz, and 20MHz offsets. Added "Measured at 1 GHz" to I_R , I_R spec condition. Removed specs I_S , I_H , I_{OD} , and I_{OE} from AC spec table. Removed ΔV_{PP} reference from Figure 4.		
*D	3135189	CXQ	01/12/2011	Changed status from Preliminary to Final. Removed "Functional equivalent" bullet on page 1. Added "(see I _{OZ})" note to pin 8 description in Pin Definitions. Fixed typo and removed resistors from IN _X /IN _X # in Logic Block Diagram. Added Figure 10 to describe T _{SOE} and T _{SOD} .		
*E	3090938	CXQ	02/25/11	Post to external web.		
*F	3208968	CXQ	03/29/2011	Changed R_P max from 140 $k\Omega$ to 165 $k\Omega$ and updated R_P in Logic Block Diagram.		
*G	3308039	CXQ	07/11/2011	Updated supported differential input clock types to include CML in Features Functional Description, Pin Definitions, and DC specs table sections.		
*H	3395868	PURU	10/05/11	Updated supported differential input clock types to include HCSL in Features Pinouts, and DC Electrical Specifications table. Changed Min value of $V_{\rm ICM}$.		
*	3892255	PURU	02/01/2013	Updated Features (Added "Translates any single-ended input signal to 3.3 LVPECL levels with resistor bias on INx# input"). Updated AC Electrical Specifications: Added Note 9 and Note 14. Added F $_{\rm IN}$ parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz). Added F $_{\rm OUT}$ parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz). Added t $_{\rm ODC}$ parameter values for "Single Ended Input" condition (Minimum value = 45%, Maximum value = 55%). Updated Description of PN $_{\rm ADD}$ parameter (Replaced "Additive RMS phasnoise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V $_{\rm ID}$ > 400 mV with "Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V $_{\rm ID}$ > 400 mV or Input Swing = 3.0 V $^{(9)}$ "). Added t $_{\rm JIT}$ parameter values for the Condition "156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V $^{(14)}$ " (Maximum value = 0.11 ps). Added Application Information. Updated to new template.		
*J	4587249	PURU	12/04/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Package Diagram: spec 51-85118 – Changed revision from *D to *E.		
*K	5267558	PSR	05/13/2016	Added Thermal Resistance. Updated to new template.		
*L	5962077	AESATMP8	11/09/2017	Updated logo and Copyright.		



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers

Automotive

Clocks & Buffers

Interface

Internet of Things

cypress.com/automotive

cypress.com/clocks

cypress.com/interface

cypress.com/interface

Memory cypress.com/memory
Microcontrollers cypress.com/mcu
PSoC cypress.com/psoc

Power Management ICs cypress.com/pmic
Touch Sensing cypress.com/touch
USB Controllers cypress.com/usb
Wireless Connectivity cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2009-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Document Number: 001-56312 Rev. *L Revised November 9, 2017 Page 16 of 16

ПОСТАВКА ЭЛЕКТРОННЫХ КОМПОНЕНТОВ

многоканальный

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001 Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9