High Isolation, Silicon SPDT, Nonreflective Switch, 0.1 GHz to 6.0 GHz

Data Sheet **HMC8038**

FEATURES

- Nonreflective, 50 Ω design
- High isolation: 60 dB typical
- Low insertion loss: 0.8 dB typical
- High power handling
  - 34 dBm through path
  - 29 dBm terminated path
- High linearity
  - 0.1 dB compression (P0.1dB): 35 dBm typical
  - Input third-order intercept (IP3): 60 dBm typical
- ESD ratings
  - 4 kV human body model (HBM), Class 3A
  - 1.25 kV charged device model (CDM)
- Single positive supply
  - 3.3 V to 5 V
  - 1.8 V-compatible control
- All off state control
- 16-lead, 4 mm × 4 mm LFCSP (16 mm²)
- Pin compatible with the HMC849ALP4CE

APPLICATIONS

- Cellular/4G infrastructure
- Wireless infrastructure
- Automotive telematics
- Mobile radios
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

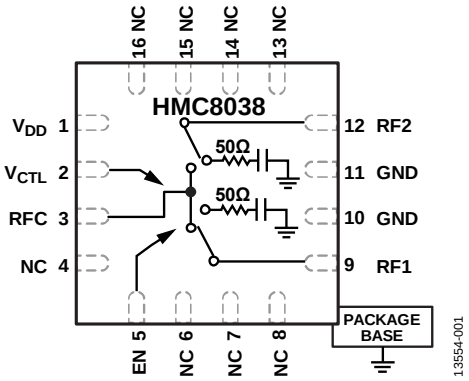

Figure 1.

GENERAL DESCRIPTION

The HMC8038 is a high isolation, nonreflective, 0.1 GHz to 6.0 GHz, silicon, single-pole, double-throw (SPDT) switch in a leadless, surface-mount package. The switch is ideal for cellular infrastructure applications, yielding up to 62 dB of isolation up to 4.0 GHz, a low 0.8 dB of insertion loss up to 4.0 GHz, and 60 dBm of input third-order intercept. Power handling is excellent up to 6.0 GHz, and it offers an input power for an 0.1 dB compression point (P0.1dB) of 35 dBm (V_{DD} = 5 V). On-chip circuitry operates a single, positive supply voltage from 3.3 V to 5 V, as well as a single, positive voltage control from 0 V to 1.8 V/3.3 V/5.0 V at very low dc currents. An enable input (EN) set to logic high places the switch in an all off state, in which RFC is reflective.

The HMC8038 has ESD protection on all device pins, including the RF interface, and can stand 4 kV HMB and 1.25 kV CDM. The HMC8038 offers very fast switching and RF settling times of 150 ns and 170 ns, respectively. The device comes in a RoHS-compliant, compact 4 mm × 4 mm LFCSP.

Rev. A
Document Feedback

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REVISION HISTORY

11/15—Rev. 0 to Rev. A

Changes to Table 1 3

9/15—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V to 5 V, V_{CTL} = 0 V/V_{DD}, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INSERTION LOSS	0.1 GHz to 2.0 GHz		0.7	1.0	dB
	2.0 GHz to 4.0 GHz		0.8	1.1	dB
	4.0 GHz to 6.0 GHz		0.9	1.3	dB
ISOLATION	0.1 GHz to 2.0 GHz	55	70		dB
RFC to RF1/RF2 (Worst Case)	2.0 GHz to 4.0 GHz	50	60		dB
	4.0 GHz to 6.0 GHz	40	51		dB
RETURN LOSS					
On State	0.1 GHz to 2.0 GHz		24		dB
	2.0 GHz to 4.0 GHz		18		dB
	4.0 GHz to 6.0 GHz		18		dB
Off State	0.1 GHz to 2.0 GHz		23		dB
	2.0 GHz to 4.0 GHz		22		dB
	4.0 GHz to 6.0 GHz		16		dB
SWITCHING SPEED					
t_{RISE}, t_{FALL}	10%/90% RF_{OUT}		60		ns
t_{ON}, t_{OFF}	50% V_{CTL} to 10%/90% RF_{OUT}		150		ns
RF SETTLING TIME	50% V_{CTL} to 0.1 dB margin of final RF_{OUT}		170		ns
INPUT POWER					
1 dB Compression (P1dB)	V_{DD} = 3.3 V		34		dB
	V_{DD} = 5 V		36		dB
0.1 dB Compression (P0.1dB)	V_{DD} = 3.3 V		33		dB
	V_{DD} = 5 V		35		dB
INPUT THIRD-ORDER INTERCEPT (IP3)	Two-tone input power = 14 dBm/tone		60		dBm
RECOMMENDED OPERATING CONDITIONS					
Bias Voltage Range (V_{DD})		3.0		5.4	V
Control Voltage Range (V_{CTL}, EN)		0		V_{DD}	V
Maximum RF Input Power[1]					
T_{CASE} = 105°C	Through Path (5 V/3.3 V)	31/30			dBm
	Terminated Path	24			dBm
	Hot Switching	24			dBm
T_{CASE} = 85°C	Through Path (5 V/3.3 V)	34/33			dBm
	Terminated Path	27			dBm
	Hot Switching	27			dBm
T_{CASE} = 25°C	Through Path (5 V/3.3 V)	34/33			dBm
	Terminated Path	29			dBm
	Hot Switching	27			dBm
T_{CASE} = −40°C	Through Path (5 V/3.3 V)	34/33			dBm
	Terminated Path	29			dBm
	Hot Switching	27			dBm
Case Temperature Range (T_{CASE})		−40		+105	°C

[1] Exposure to levels between the recommended operating conditions and the absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Digital Control Voltages

State	V_{DD} = 3.3 V (±5% V_{DD}, T_{CASE} = −40°C to +105°C)	V_{DD} = 5 V (±5% V_{DD}, T_{CASE} = −40°C to +105°C)
Input Control Voltage		
Low (V_{IL})	0 V to 0.85 V at <1 µA, typical	0 V to 1.20 V at <1 µA, typical
High (V_{IH})	1.15 V to 3.3 V at <1 µA, typical	1.55 V to 5.0 V at <1 µA, typical

Table 3. Bias Voltage vs. Supply Current

Parameter	Symbol	Min	Typ	Max	Unit	Typical I_{DD} (mA)
SUPPLY CURRENT	I_{DD}					
V_{DD} = 3.3 V			0.14		mA	0.14
V_{DD} = 5 V			0.16		mA	0.16

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Bias Voltage Range (V_{DD})	−0.3 V to +5.5 V
Control Voltage Range (V_{CTL}, EN)	−0.5 V to V_{DD} + (+0.5 V)
RF Input Power[1] (see Figure 2)	
Through Path	35 dBm
Terminated Path	30 dBm
Hot Switching	30 dBm
Channel Temperature	135°C
Storage Temperature Range	−65°C to +150°C
Thermal Resistance (Channel to Package Bottom)	
Through Path	110°C/W
Terminated Path	100°C/W
ESD Sensitivity	
HBM	4 kV (Class 3A)
CDM	1.25 kV

[1] For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

During the through mode of operation, the supply voltage scales the maximum allowed input power. The power handling vs. frequency for the 3.3 V and 5 V supplies is shown in Figure 2.

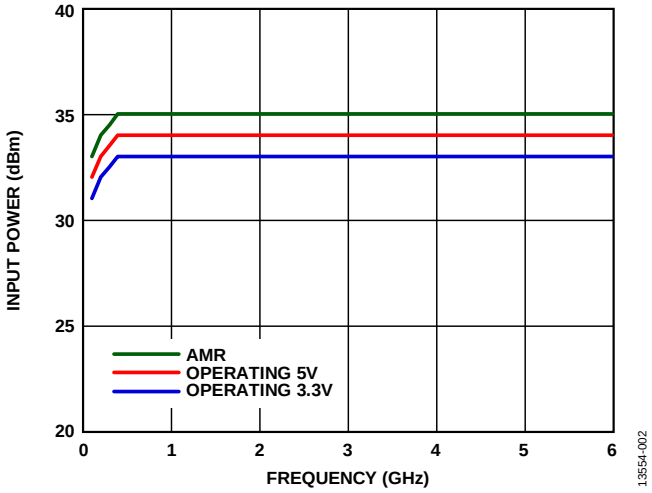

Figure 2. Through Path, Power Handling vs. Frequency

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

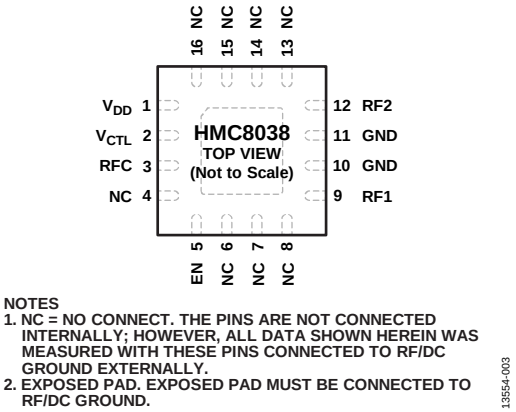

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Supply Voltage Pin.
2	V_{CTL}	Control Input Pin. See Figure 5 for the V_{CTL} interface schematic. Refer to Table 6 and the recommended input control voltage range in Table 2.
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
4, 6 to 8, 13 to 16	NC	Not Internally Connected. These pins are not internally connected; however, all data shown in this data sheet is measured with the NC pins externally connected to RF/dc ground on the evaluation board.
5	EN	Enable Input Pin. See Figure 5 for the EN interface schematic. Refer to Table 6 and the recommended input control voltage range in Table 2.
9	RF1	RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
10, 11	GND	Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF ground. See Figure 4 for the GND interface schematic.
12	RF2	RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
	EPAD	Exposed Pad. Exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 4. GND Interface Schematic

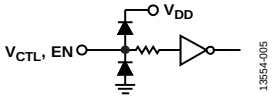

Figure 5. Logic Control Interface Schematic

Table 6. Truth Table

Control Input		Signal Path State	
V_{CTL} State	EN State	RFC to RF1	RFC to RF2
Low	Low	Off	On
High	Low	On	Off
Low	High	Off	Off
High	High	Off	Off

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

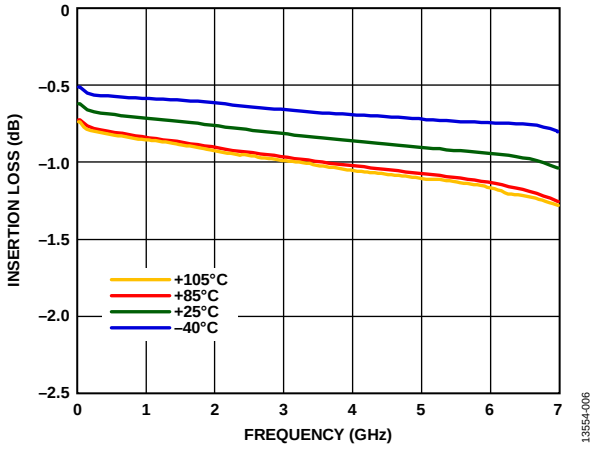

Figure 6. Insertion Loss vs. Frequency over Temperatures, V_{DD} = 5 V

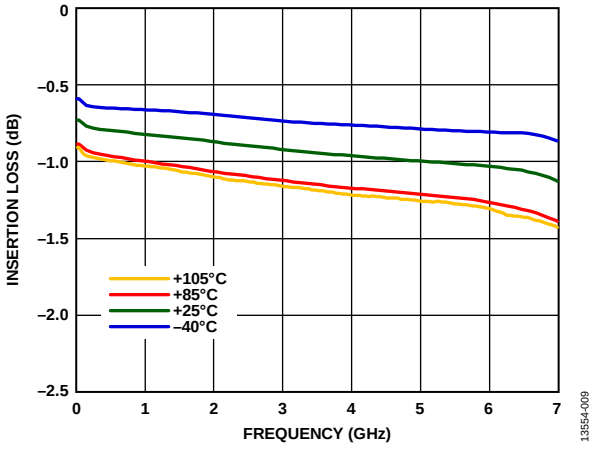

Figure 9. Insertion Loss vs. Frequency over Temperatures, V_{DD} = 3.3 V

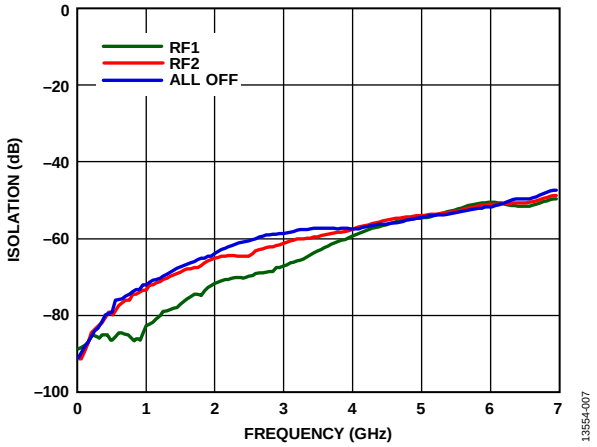

Figure 7. Isolation Between RFC and RF1/RF2 vs. Frequency at V_{DD} = 3.3 V to 5 V

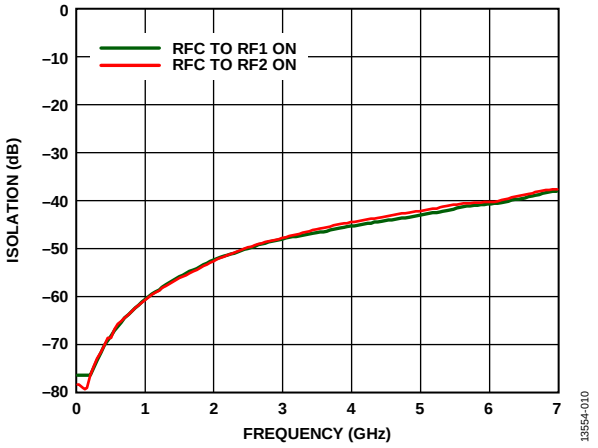

Figure 10. Isolation Between RF1 and RF2 vs. Frequency at V_{DD} = 3.3 V to 5 V

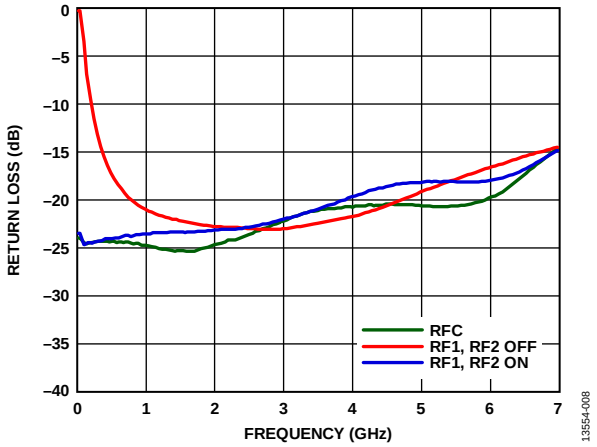

Figure 8. Return Loss vs. Frequency at V_{DD} = 3.3 V to 5 V

INPUT COMPRESSION AND INPUT THIRD-ORDER INTERCEPT

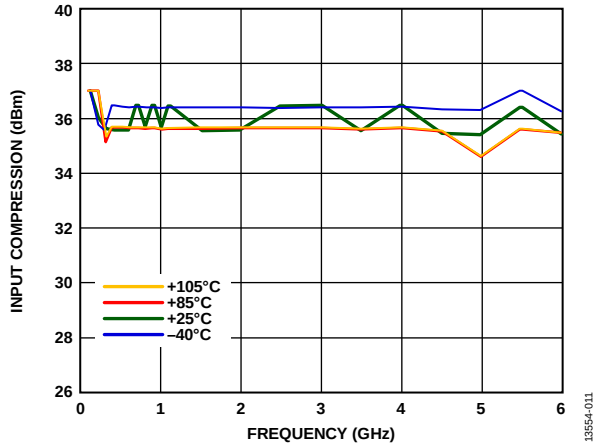

Figure 11. Input Compression 1 dB Point vs. Frequency over Temperature, V_{DD} = 5 V

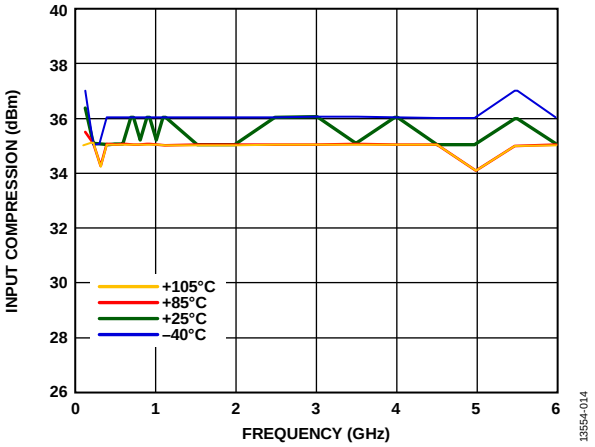

Figure 14. Input Compression 0.1 dB Point vs. Frequency over Temperature, V_{DD} = 5 V

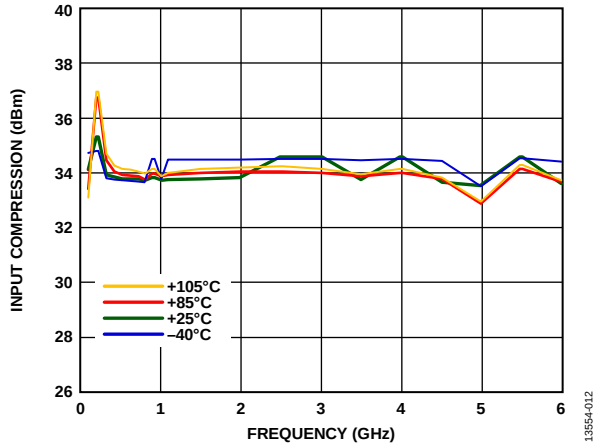

Figure 12. Input Compression 1 dB Point vs. Frequency over Temperature, V_{DD} = 3.3 V

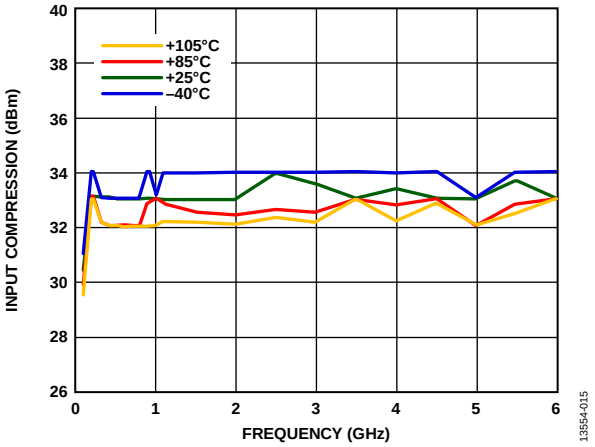

Figure 15. Input Compression 0.1 dB Point vs. Frequency over Temperature, V_{DD} = 3.3 V

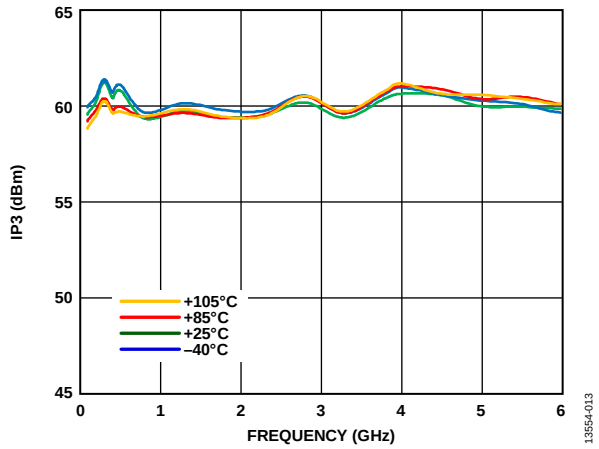

Figure 13. Input Third-Order Intercept (IP3) Point vs. Frequency, V_{DD} = 5 V

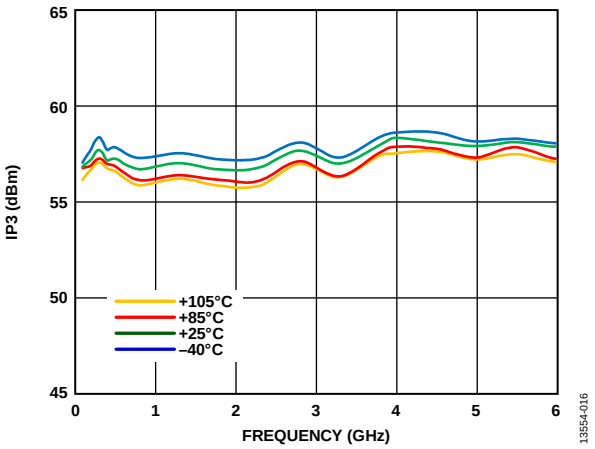

Figure 16. Input Third-Order Intercept (IP3) Point vs. Frequency, V_{DD} = 3.3 V

THEORY OF OPERATION

The HMC8038 requires a single-supply voltage applied to the V_{DD} pin. Bypassing capacitors are recommended on the supply line to minimize RF coupling.

The HMC8038 is controlled via two digital control voltages applied to the V_{CTL} pin and the EN pin. A small bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The HMC8038 is internally matched to 50 Ω at the RF input port (RFC) and the RF output ports (RF1 and RF2); therefore, no external matching components are required. The RFx pins are dc-coupled, and dc blocking capacitors are required on the RF lines. The design is bidirectional; the input and outputs are interchangeable.

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up V_{DD}.
3. Power up the digital control inputs. The relative order of the logic control inputs are not important. Powering the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage ESD protection structures.
4. Power up the RF input.

With the EN pin is logic low, the HMC8038 has two operation modes: on and off. Depending on the logic level applied to the V_{CTL} pin, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path is provided from the input to the output, as the other RF output port (for example, RF2) is set to off mode, by which the output is isolated from the input. When the RF output port (RF1 or RF2) is in isolation mode, internally terminate it to 50 Ω, and the port absorbs the applied RF signal.

When the EN pin is logic high, the EN pin sets the HMC8038 switch to off mode. In off mode, both output ports are isolated from the input, and the RFC port is open reflective.

Table 7. Switch Operation Mode

Digital Control Inputs		Switch Mode	
V_{EN}	V_{CTL}	RFC to RF1	RFC to RF2
0	0	Off mode. The RF1 port is isolated from the RFC port and is internally terminated to a 50 Ω load to absorb the applied RF signals.	On mode. A low insertion loss path from the RFC port to the RF2 port.
0	1	On mode. A low insertion loss path from the RFC port to the RF1 port.	Off mode. The RF2 port is isolated from the RFC port and is internally terminated to a 50 Ω load to absorb the applied RF signals.
1	X[1]	All in off mode. Both the RF1 and RF2 ports are isolated from the RFC port, and the RFC port is reflective.	

[1] X stands for don't care.

APPLICATIONS INFORMATION

Generate the evaluation PCB used in the application shown in Figure 17 with proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and backside ground slug must connect directly to the ground plane, as shown in Figure 18. The evaluation board shown in Figure 18 is available from Analog Devices, Inc. upon request.

Table 8. Bill of Materials for Evaluation Board EV1HMC8038LP4C[1]

Reference Designator	Description
J1 to J3	PCB mount SMA connector
C1 to C6	100 pF capacitor, 0402 package
C7	0.1 µF capacitor, 0402 package
R1, R2	0 Ω resistor, 0402 package
U1	HMC8038 SPDT switch
PCB[2]	600-01267-00 evaluation PCB

[1] Reference to this evaluation board number when ordering the complete evaluation board.
[2] Circuit board material: Roger 4350 or Arlon 25FR.

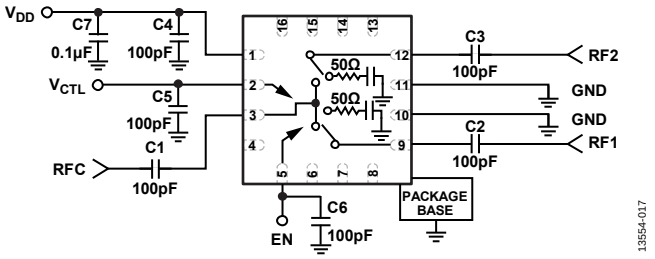

Figure 17. HMC8038 Application Circuit

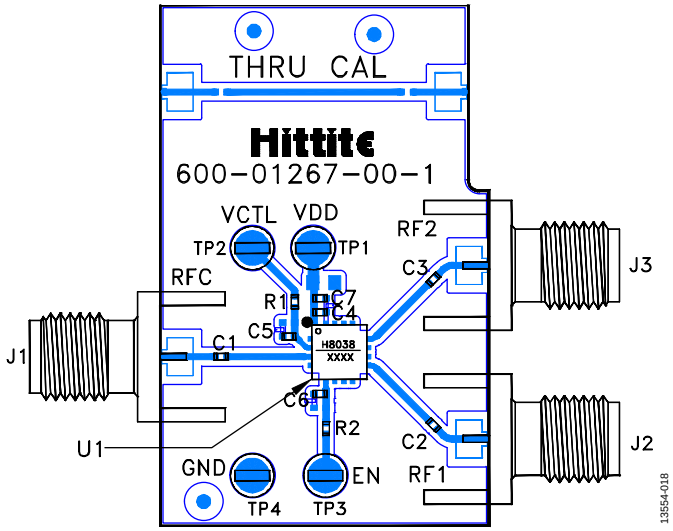

Figure 18. EV1HMC8038LP4C Evaluation Board

OUTLINE DIMENSIONS

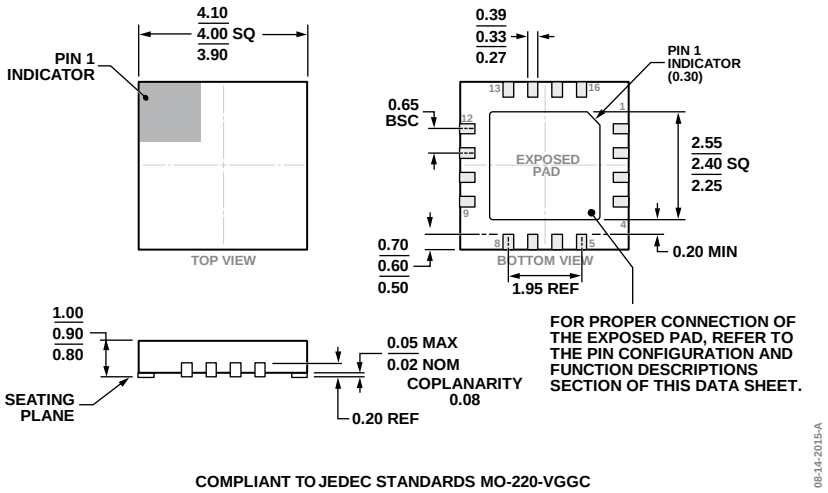

Figure 19. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.90 mm Package Height
(CP-16-40)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option	Branding[3]
HMC8038LP4CE	−40°C to +105°C	MSL3	16-lead Lead Frame Chip Scale Package [LFCSP]	CP-16-40	8038 XXXX
HMC8038LP4CETR	−40°C to +105°C	MSL3	16-lead Lead Frame Chip Scale Package [LFCSP]	CP-16-40	8038 XXXX
EV1HMC8038LP4C	−40°C to +105°C		Evaluation Board		

[1] RoHs-Compliant Part.
[2] The maximum peak reflow temperature is 260°C.
[3] 4-digit lot number: XXXX.

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