

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## General Description

The MAX5391/MAX5393 dual 256-tap, volatile, low-voltage linear taper digital potentiometers offer three end-to-end resistance values of 10k $\Omega$ , 50k $\Omega$ , and 100k $\Omega$ . Operating from a single +1.7V to +5.5V power supply, these devices provide a low 35ppm/ $^{\circ}$ C end-to-end temperature coefficient. The devices feature an SPI™ interface.

The small package size, low supply voltage, low supply current, and automotive temperature range of the MAX5391/MAX5393 make the devices uniquely suitable for the portable consumer market, battery backup industrial applications, and the automotive market.

The MAX5391/MAX5393 include two digital potentiometers in a voltage-divider configuration. The MAX5391/MAX5393 are specified over the -40 $^{\circ}$ C to +125 $^{\circ}$ C automotive temperature range and are available in a 16-pin, 3mm x 3mm TQFN and a 14-pin TSSOP package, respectively.

## Applications

Low-Voltage Battery Applications  
 Portable Electronics  
 Mechanical Potentiometer Replacement  
 Offset and Gain Control  
 Adjustable Voltage References/Linear Regulators  
 Automotive Electronics

## Features

- ◆ Dual 256-Tap Linear Taper Positions
- ◆ Single +1.7V to +5.5V Supply Operation
- ◆ Low 12 $\mu$ A Quiescent Supply Current
- ◆ 10k $\Omega$ , 50k $\Omega$ , and 100k $\Omega$  End-to-End Resistance Values
- ◆ SPI-Compatible Interface
- ◆ Wiper Set to Midscale on Power-Up
- ◆ -40 $^{\circ}$ C to +125 $^{\circ}$ C Operating Temperature Range

## Ordering Information

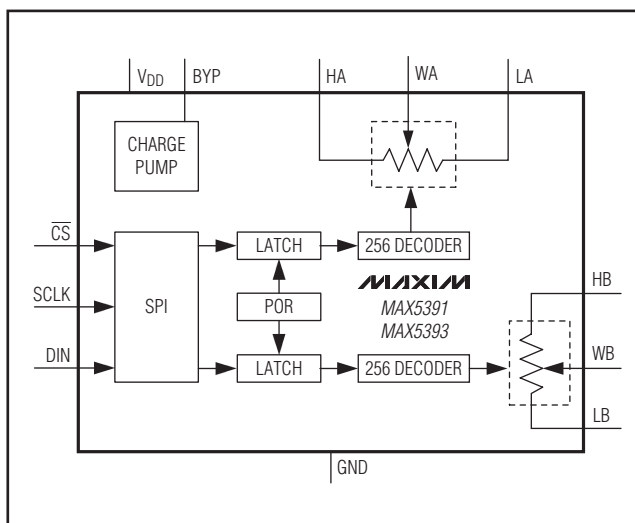
PART	PIN-PACKAGE	END-TO-END RESISTANCE (k $\Omega$ )
MAX5391LATE+	16 TQFN-EP*	10
MAX5391MATE+	16 TQFN-EP*	50
MAX5391NATE+	16 TQFN-EP*	100
MAX5393LAUD+	14 TSSOP	10
MAX5393MAUD+	14 TSSOP	50
MAX5393NAUD+	14 TSSOP	100

**Note:** All devices are specified in the -40 $^{\circ}$ C to +125 $^{\circ}$ C temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

## Functional Diagram



SPI is a trademark of Motorola, Inc.

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND .....	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
H <sub>-</sub> , W <sub>-</sub> , L <sub>-</sub> to GND .....	-0.3V to the lower of (V <sub>DD</sub> + 0.3V) or +6V	14-Pin TSSOP (derate 10mW/°C above +70°C) ..... 796.8mW
All Other Pins to GND .....	-0.3V to +6V	16-Pin TQFN (derate 14.7mW/°C above +70°C) ... 1176.5mW
Continuous Current into H <sub>-</sub> , W <sub>-</sub> , and L <sub>-</sub>		Operating Temperature Range .....
MAX5391L/MAX5393L .....	±5mA	-40°C to +125°C
MAX5391M/MAX5393M .....	±2mA	Junction Temperature .....
MAX5391N/MAX5393N .....	±1mA	+150°C
		Storage Temperature Range.....
		-65°C to +150°C
		Lead Temperature (soldering, 10s) .....
		+300°C
		Soldering Temperature (reflow) .....
		+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +1.7V to +5.5V, V<sub>H-</sub> = V<sub>DD</sub>, V<sub>L-</sub> = 0, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>DD</sub> = +1.8V, T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N		256			Tap
<b>DC PERFORMANCE (Voltage-Divider Mode)</b>						
Integral Nonlinearity	INL	(Note 2)	-0.5		+0.5	LSB
Differential Nonlinearity	DNL	(Note 2)	-0.5		+0.5	LSB
Dual-Code Matching		Register A = Register B	-0.5		+0.5	LSB
Ratiometric Resistor Tempco		( $\Delta V_W/V_W$ )/ $\Delta T$ , no load		5		ppm/°C
Full-Scale Error	Code = FFh	MAX5391L/MAX5393L	-3	-2.2		LSB
		MAX5391M/MAX5393M	-1	-0.6		
		MAX5391N/MAX5393N	-0.5	-0.3		
Zero-Scale Error	Code = 00h	MAX5391L/MAX5393L		2.2	3	LSB
		MAX5391M/MAX5393M		0.6	1	
		MAX5391N/MAX5393N		0.3	0.5	
<b>DC PERFORMANCE (Variable Resistor Mode)</b>						
Integral Nonlinearity (Note 3)	R-INL	MAX5391L/MAX5393L	-1.5		+1.5	LSB
		MAX5391M/MAX5393M	-0.75		+0.75	
		MAX5391N/MAX5393N	-0.5		+0.5	
Differential Nonlinearity	R-DNL	(Note 3)	-0.5		+0.5	LSB
<b>DC PERFORMANCE (Resistor Characteristics)</b>						
Wiper Resistance	R <sub>WL</sub>	(Note 4)			200	Ω
Terminal Capacitance	C <sub>H-</sub> , C <sub>L-</sub>	Measured to GND		10		pF
Wiper Capacitance	C <sub>W-</sub>	Measured to GND		50		pF
End-to-End Resistor Tempco	TCR	No load		35		ppm/°C
End-to-End Resistor Tolerance	ΔR <sub>HL</sub>	Wiper not connected	-25		+25	%
<b>AC PERFORMANCE</b>						
Crosstalk		(Note 5)		-90		dB
-3dB Bandwidth	BW	Code = 80H, 10pF load, V <sub>DD</sub> = 1.8V	MAX5391L/MAX5393L	600		kHz
			MAX5391M/MAX5393M	100		
			MAX5391N/MAX5393N	50		
Total Harmonic Distortion Plus Noise	THD+N	Measured at W, V <sub>H-</sub> = 1V <sub>RMS</sub> at 1kHz		0.02		%

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

MAX5391/MAX5393

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = +1.7V to +5.5V, V<sub>H</sub> = V<sub>DD</sub>, V<sub>L</sub> = 0, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>DD</sub> = +1.8V, T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Wiper Settling Time (Note 6)	t <sub>S</sub>	MAX5391L/MAX5393L		400		ns
		MAX5391M/MAX5393M		1200		
		MAX5391N/MAX5393N		2200		
Charge-Pump Feedthrough at W <sub>-</sub>	V <sub>RW</sub>	f <sub>CLK</sub> = 600kHz, C <sub>OUT</sub> = 0nF		200		nV <sub>P-P</sub>
<b>POWER SUPPLIES</b>						
Supply Voltage Range	V <sub>DD</sub>		1.7		5.5	V
Standby Current		V <sub>DD</sub> = 5.5V	27			μA
		V <sub>DD</sub> = 1.7V	12			
<b>DIGITAL INPUTS</b>						
Minimum Input High Voltage	V <sub>IH</sub>	V <sub>DD</sub> = 2.6V to 5.5V	70			% × V <sub>DD</sub>
		V <sub>DD</sub> = 1.7V to 2.6V	75			
Maximum Input Low Voltage	V <sub>IL</sub>	V <sub>DD</sub> = 2.6V to 5.5V			30	% × V <sub>DD</sub>
		V <sub>DD</sub> = 1.7V to 2.6V			25	
Input Leakage Current			-1		+1	μA
Input Capacitance				5		pF
<b>TIMING CHARACTERISTICS—SPI (Note 7)</b>						
SCLK Frequency	f <sub>MAX</sub>				10	MHz
SCLK Clock Period	t <sub>CP</sub>		100			ns
SCLK Pulse-Width High	t <sub>CH</sub>		40			ns
SCLK Pulse-Width Low	t <sub>CL</sub>		40			ns
$\overline{\text{CS}}$ Fall to SCK Rise Setup Time	t <sub>CSS</sub>		40			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	t <sub>CSH</sub>		0			ns
DIN Setup Time	t <sub>DS</sub>		40			ns
DIN Hold Time	t <sub>DH</sub>		0			ns
SCLK Rise to $\overline{\text{CS}}$ Fall Delay	t <sub>CS0</sub>		10			ns
SCLK Rise to SCLK Rise Hold Time	t <sub>CS1</sub>		40			ns
$\overline{\text{CS}}$ Pulse-Width High	t <sub>CSW</sub>		100			ns

**Note 1:** All devices are 100% production tested at T<sub>A</sub> = +25°C. Specifications over temperature limits are guaranteed by design and characterization.

**Note 2:** DNL and INL are measured with the potentiometer configured as a voltage-divider (Figure 1) with H<sub>-</sub> = V<sub>DD</sub> and L<sub>-</sub> = GND. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

**Note 3:** R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). DNL and INL are measured with the potentiometer configured as a variable resistor. H<sub>-</sub> is unconnected and L<sub>-</sub> = GND. For V<sub>DD</sub> = +5V, the wiper terminal is driven with a source current of 400μA for the 10kΩ configuration, 80μA for the 50kΩ configuration, and 40μA for the 100kΩ configuration. For V<sub>DD</sub> = +1.7V, the wiper terminal is driven with a source current of 150μA for the 10kΩ configuration, 30μA for the 50kΩ configuration, and 15μA for the 100kΩ configuration.

**Note 4:** The wiper resistance is the value measured by injecting the currents given in Note 3 into W<sub>-</sub> with L<sub>-</sub> = GND.  
 $R_{W-} = (V_{W-} - V_{H-})/I_{W-}$

**Note 5:** Drive HA with a 1kHz GND to V<sub>DD</sub> amplitude tone. LA = LB = GND. No load. WB is at midscale with a 10pF load. Measure WB.

**Note 6:** The wiper-settling time is the worst-case 0 to 50% rise time, measured between tap 0 and tap 127. H<sub>-</sub> = V<sub>DD</sub>, L<sub>-</sub> = GND, and the wiper terminal is loaded with 10pF capacitance to ground.

**Note 7:** Digital timing is guaranteed by design and characterization, not production tested.

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

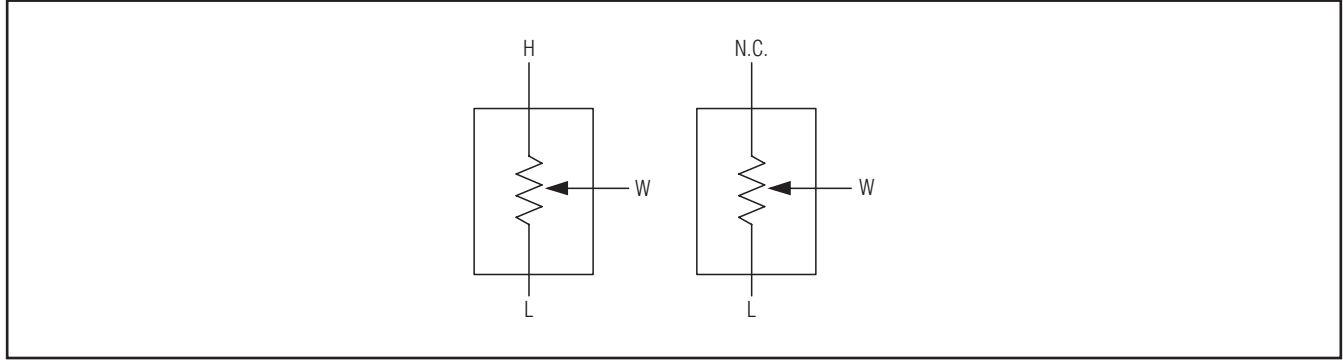
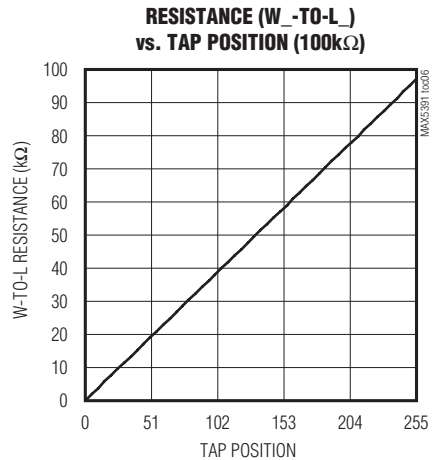
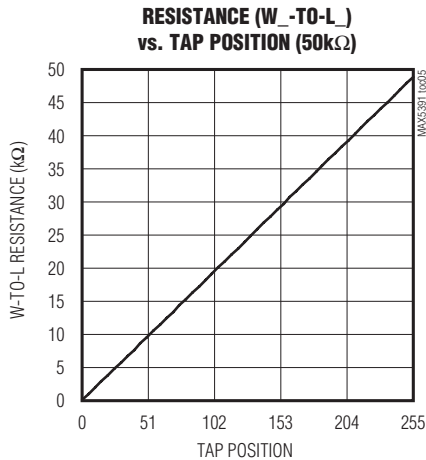
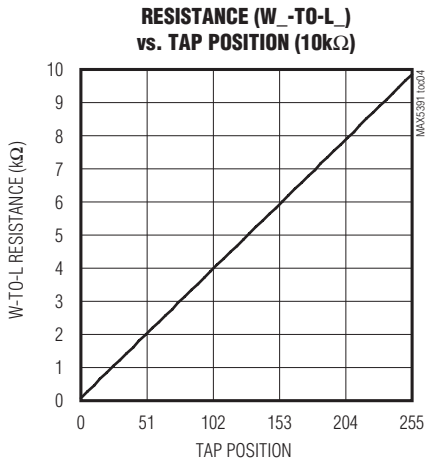
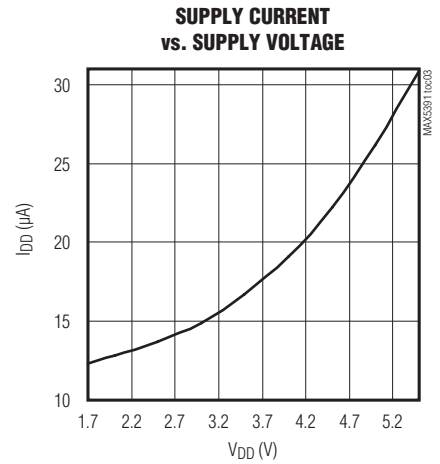
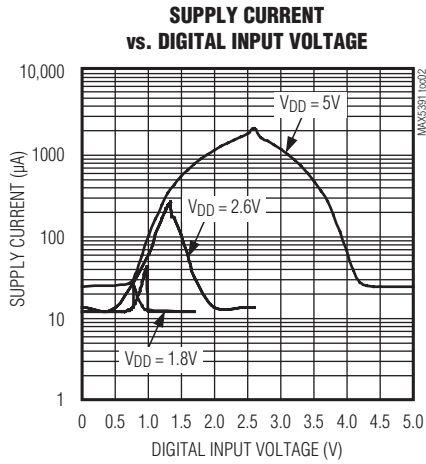
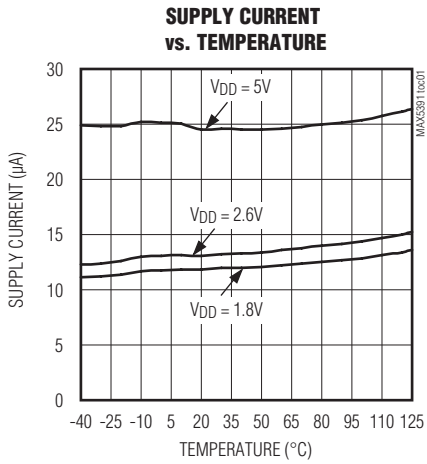


Figure 1. Voltage-Divider and Variable Resistor Configurations

## Typical Operating Characteristics

( $V_{DD} = 1.8V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

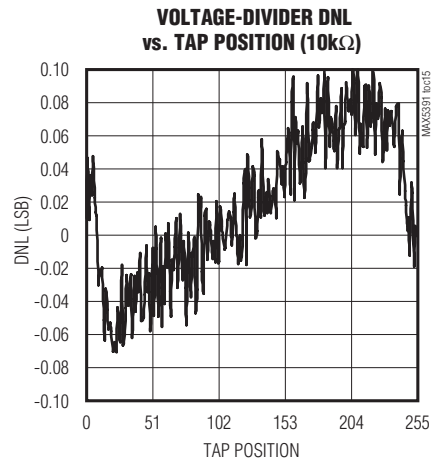
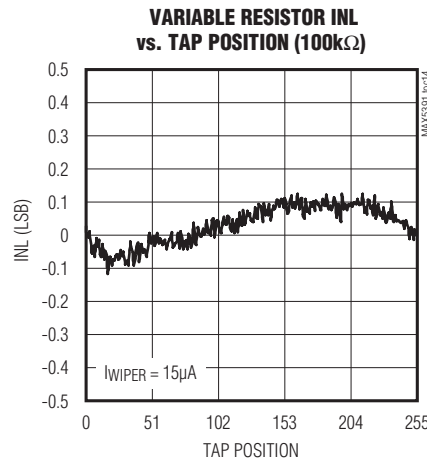
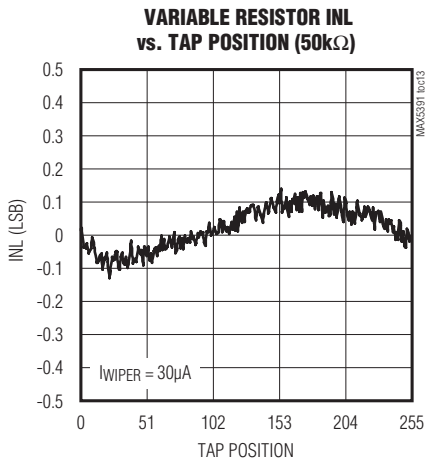
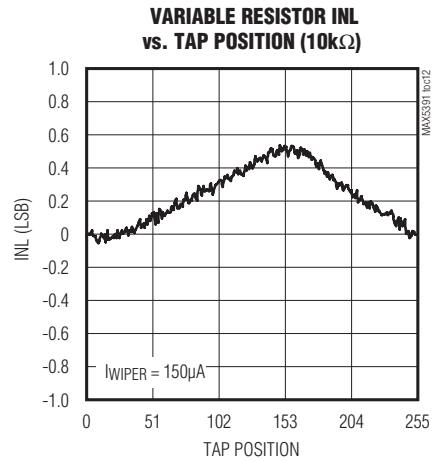
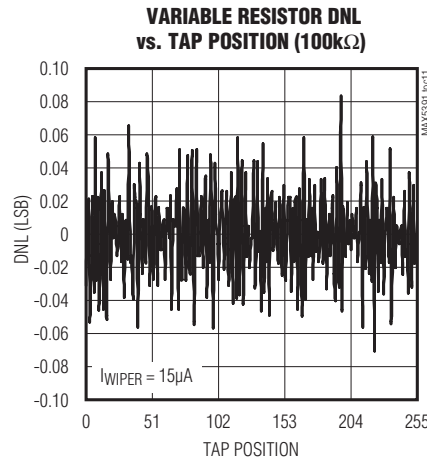
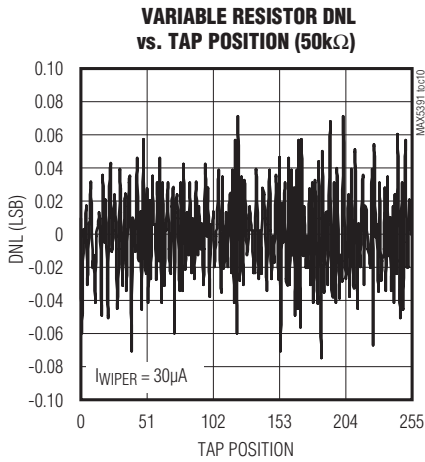
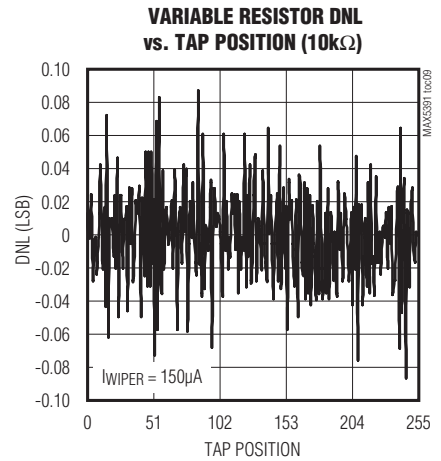
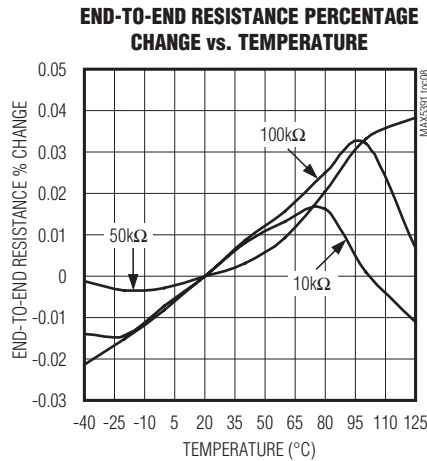
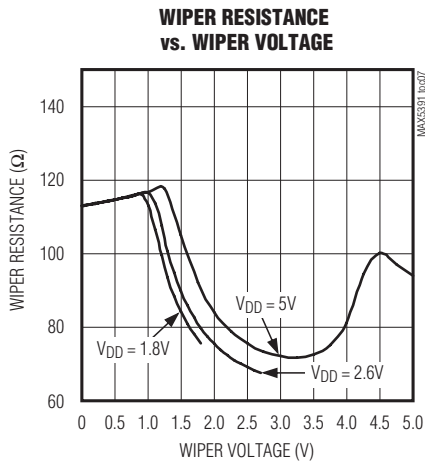


# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Typical Operating Characteristics (continued)

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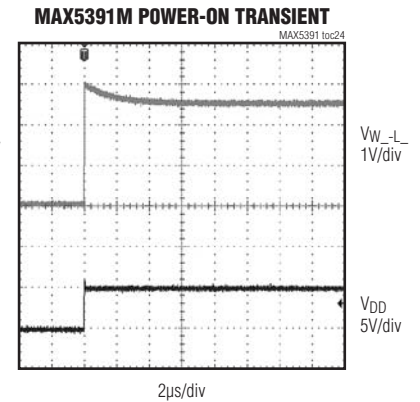
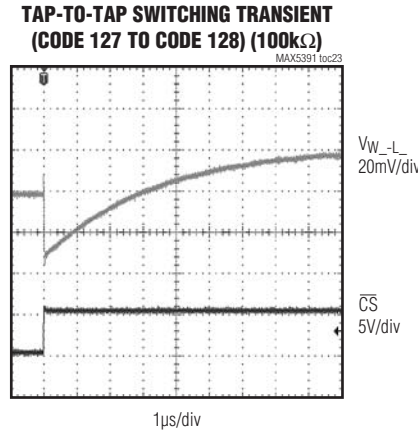
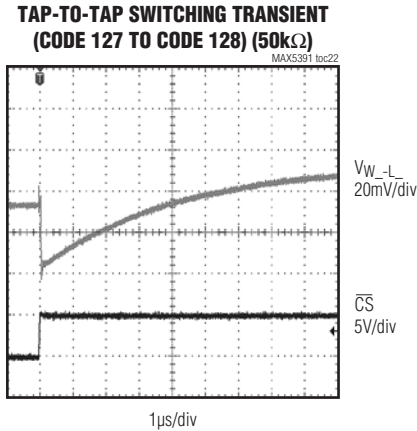
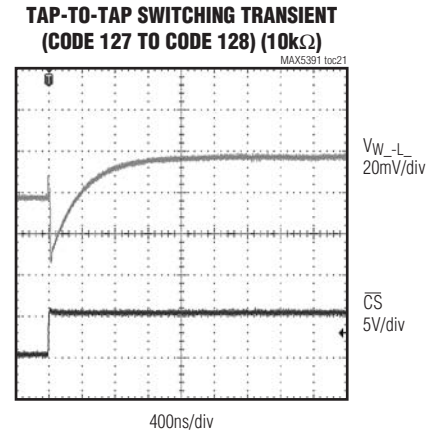
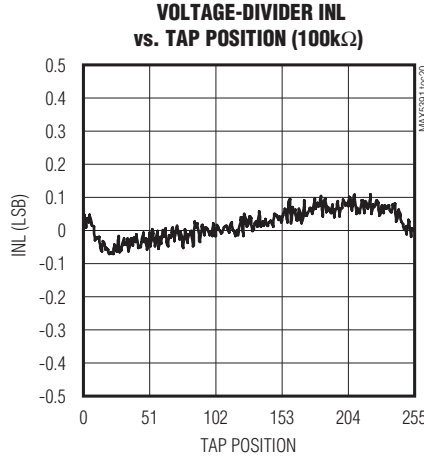
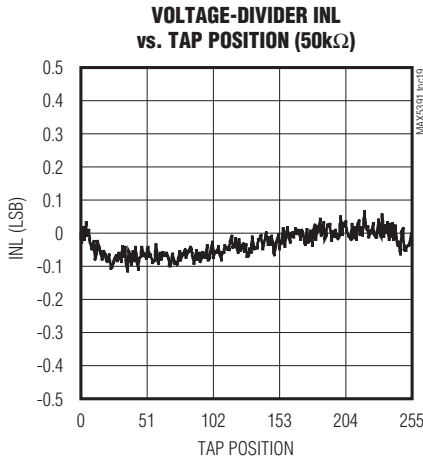
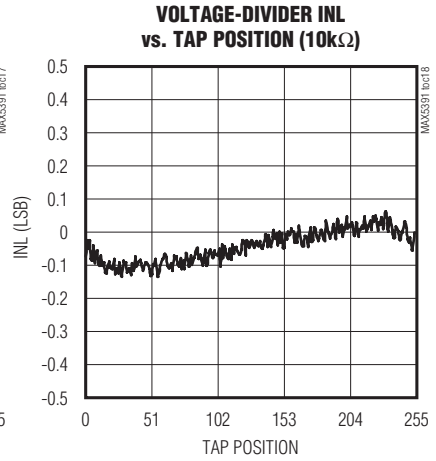
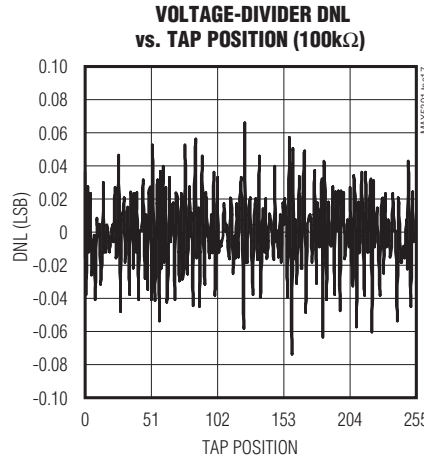
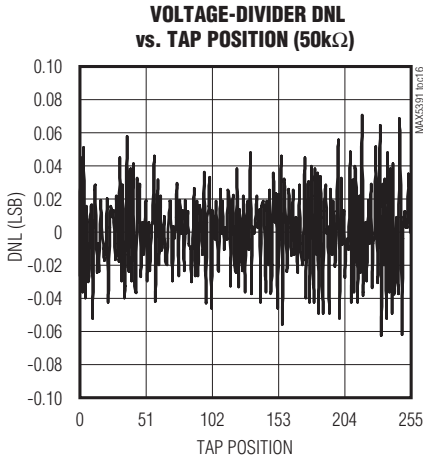
MAX5391/MAX5393



# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Typical Operating Characteristics (continued)

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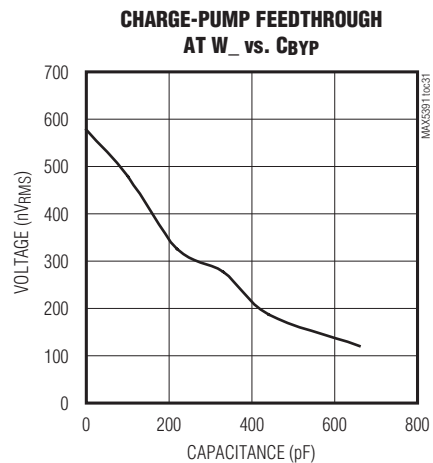
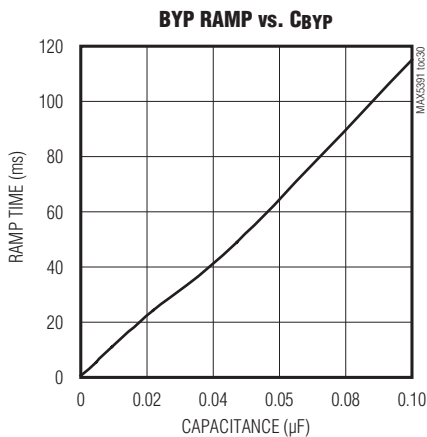
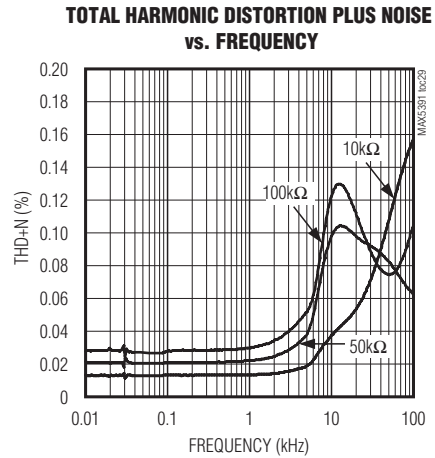
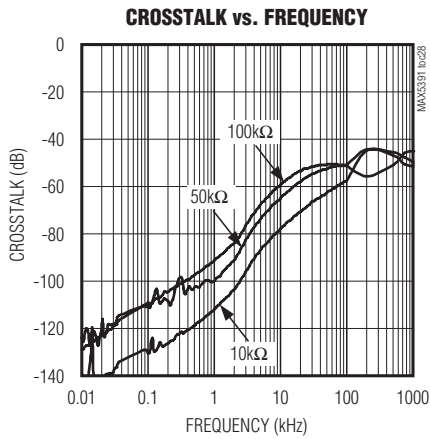
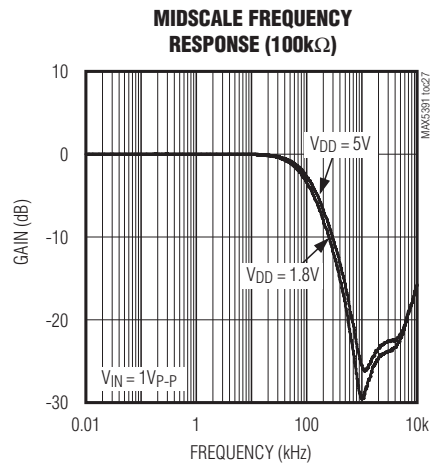
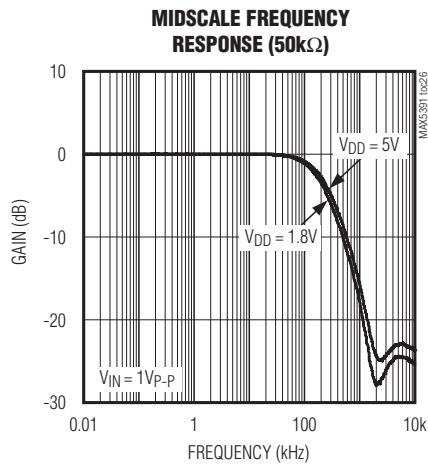
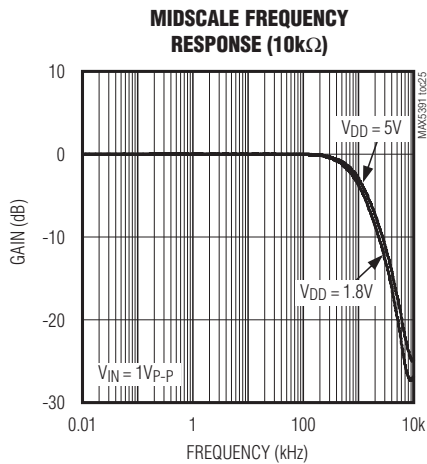


# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Typical Operating Characteristics (continued)

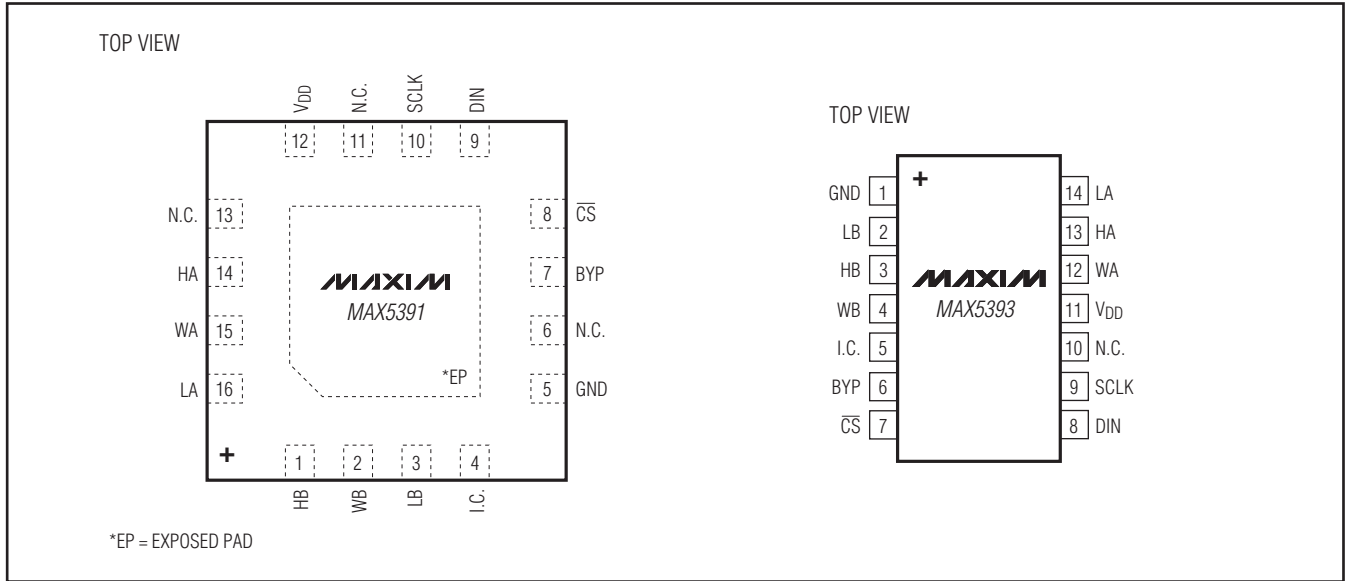
( $V_{DD} = 1.8V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX5391/MAX5393



# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Pin Configurations



## Pin Description

PIN		NAME	FUNCTION
MAX5391 (TQFN-EP)	MAX5393 (TSSOP)		
1	3	HB	Resistor B High Terminal. The voltage at HB can be higher or lower than the voltage at LB. Current can flow into or out of HB.
2	4	WB	Resistor B Wiper Terminal
3	2	LB	Resistor B Low Terminal. The voltage at LB can be higher or lower than the voltage at HB. Current can flow into or out of LB.
4	5	I.C.	Internally Connected. Connect to GND.
5	1	GND	Ground
6, 11, 13	10	N.C.	No Connection. Not internally connected.
7	6	BYP	Internal Power-Supply Bypass. For additional charge-pump filtering, bypass to GND with a capacitor close to the device.
8	7	$\overline{CS}$	Active-Low Chip-Select Input
9	8	DIN	Serial-Interface Data Input
10	9	SCLK	Serial-Interface Clock Input
12	11	VDD	Power-Supply Input. Bypass VDD to GND with a 0.1 $\mu$ F capacitor close to the device.
14	13	HA	Resistor A High Terminal. The voltage at HA can be higher or lower than the voltage at LA. Current can flow into or out of HA.
15	12	WA	Resistor A Wiper Terminal
16	14	LA	Resistor A Low Terminal. The voltage at LA can be higher or lower than the voltage at HA. Current can flow into or out of LA.
—	—	EP	Exposed Pad (MAX5391 Only). Connect to GND.



# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Detailed Description

The MAX5391/MAX5393 dual 256-tap, volatile, low-voltage linear taper digital potentiometers offer three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. Each potentiometer consists of 255 fixed resistors in series between terminals H<sub>-</sub> and L<sub>-</sub>. The potentiometer wiper, W<sub>-</sub>, is programmable to access any one of the 256 tap points on the resistor string.

The potentiometers in each device are programmable independently of each other. The MAX5391/MAX5393 feature an SPI interface.

## Charge Pump

The MAX5391/MAX5393 contain an internal charge pump that guarantees the maximum wiper resistance, R<sub>WL</sub>, to be less than 200Ω for supply voltages down to 1.7V. Pins H<sub>-</sub>, W<sub>-</sub>, and L<sub>-</sub> are still required to be less than V<sub>DD</sub> + 0.3V. A bypass input, BYP, is provided to allow additional filtering of the charge-pump output, further reducing clock feed through that may occur on H<sub>-</sub>, W<sub>-</sub>, or L<sub>-</sub>. The nominal clock rate of the charge pump is 600kHz. BYP should remain resistively unloaded as any additional load would produce a ripple of approximately I<sub>BYP</sub>/(600kHz x C<sub>BYP</sub>) volts. See the Charge-Pump Feedthrough at W<sub>-</sub> vs. C<sub>BYP</sub> graph in the *Typical Operating Characteristics* for C<sub>BYP</sub> sizing guidelines with respect to clock feedthrough to the wiper. The value of

C<sub>BYP</sub> does affect the startup time of the charge pump; however, C<sub>BYP</sub> does not impact the ability to communicate with the device, nor is there a minimum C<sub>BYP</sub> requirement. The maximum wiper impedance specification is not guaranteed until the charge pump is fully settled. See the BYP Ramp vs. C<sub>BYP</sub> graph in the *Typical Operating Characteristics* for C<sub>BYP</sub> impact on charge-pump settling time.

## SPI Digital Interface

The MAX5391/MAX5393 include a SPI interface that provides a 3-wire write-only serial-data interface to control the wiper tap position through inputs chip select ( $\overline{CS}$ ), data in (DIN), and data clock (SCLK). Drive  $\overline{CS}$  low to load data from DIN synchronously into the serial shift register on the rising edge of each SCLK pulse. The MAX5391/MAX5393 load the last 10 bits of clocked data into the appropriate potentiometer control register once  $\overline{CS}$  transitions high. See Figures 2 and 3. Data written to a memory register immediately updates the wiper position. Keep  $\overline{CS}$  low during the entire data stream to prevent the data from being terminated.

The first two bits A1:A0 (address bits) address one of the two potentiometers. See Table 1. The power-on reset (POR) circuitry sets the wiper to midscale.

**Table 1. SPI Register Map**

Bit Number	1	2	3	4	5	6	7	8	9	10
Bit Name	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register A	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register B	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write to Both A and B	1	1	D7	D6	D5	D4	D3	D2	D1	D0

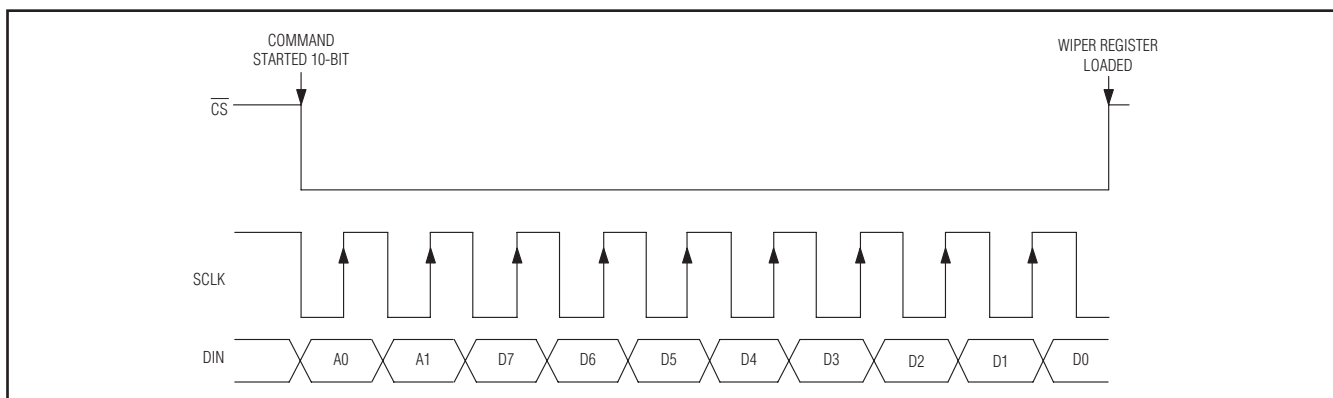


Figure 2. SPI Digital Interface Format

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

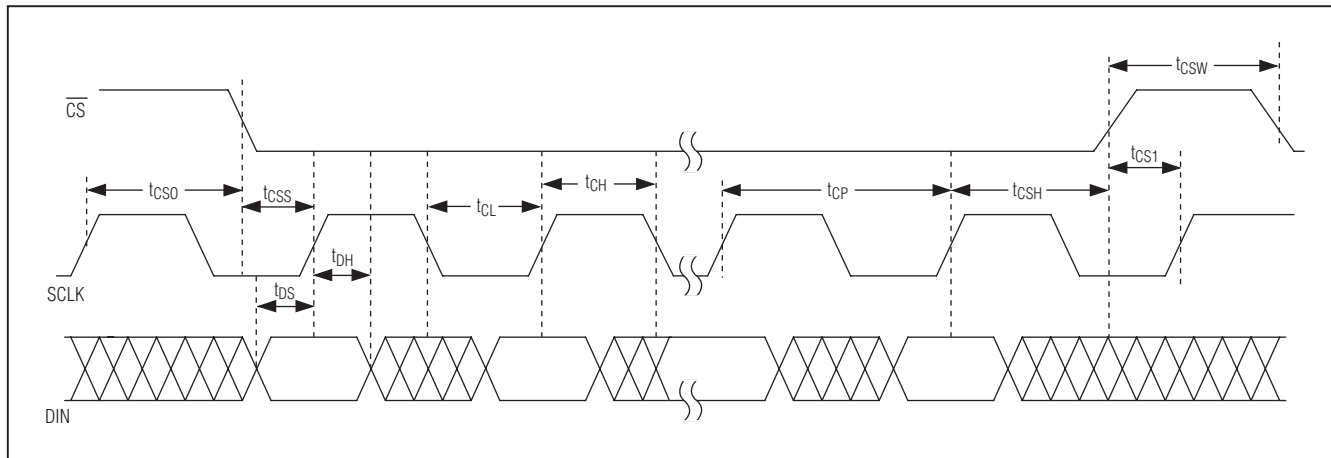


Figure 3. SPI Timing Diagram

**REG A:** The data byte writes to register A, and the wiper of potentiometer A moves to the appropriate position at the rising edge of  $\overline{CS}$ . D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to LA. D[7:0] = FFh moves the wiper closest to HA. D[7:0] is 80h following power-on.

**REG B:** The data byte writes to register B, and the wiper of potentiometer B moves to the appropriate position at the rising edge of  $\overline{CS}$ . D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to LB. D[7:0] = FFh moves the wiper to the position closest to HB. D[7:0] is 80h following power-on.

**REG A and B:** The data byte writes to registers A and B, and the wipers of potentiometers A and B move to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to L\_. D[7:0] = FFh moves the wiper to the position closest to H\_. D[7:0] is 80h following power-on.

## Applications Information

### Variable Gain Amplifier

Figure 4 shows a potentiometer adjusting the gain of a noninverting amplifier. Figure 5 shows a potentiometer adjusting the gain of an inverting amplifier.

### Adjustable Dual Regulator

Figure 6 shows an adjustable dual linear regulator using a dual potentiometer as two variable resistors.

### Adjustable Voltage Reference

Figure 7 shows an adjustable voltage reference circuit using a potentiometer as a voltage divider.

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

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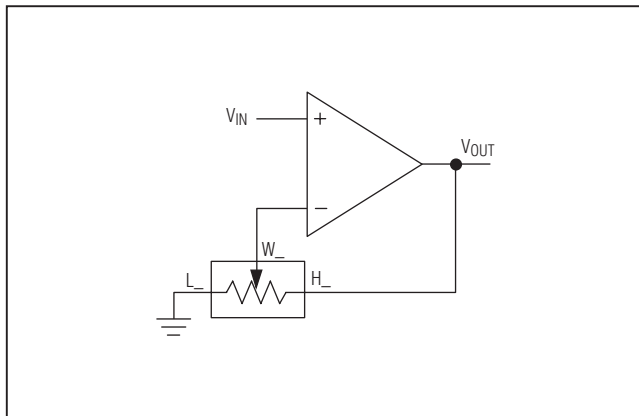


Figure 4. Variable-Gain Noninverting Amplifier

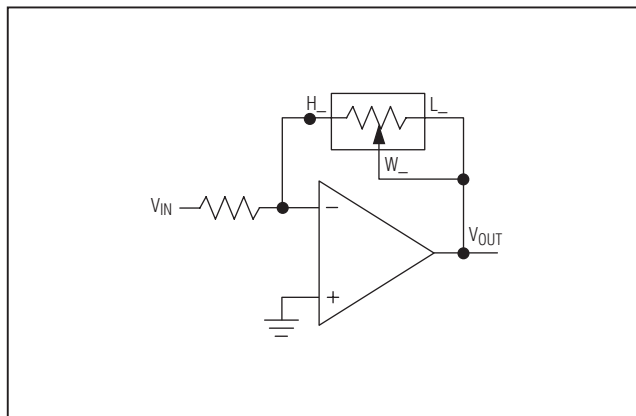


Figure 5. Variable-Gain Inverting Amplifier

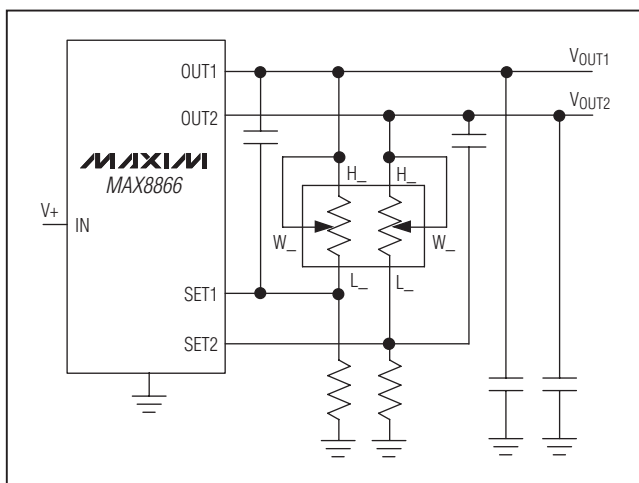


Figure 6. Adjustable Dual Linear Regulator

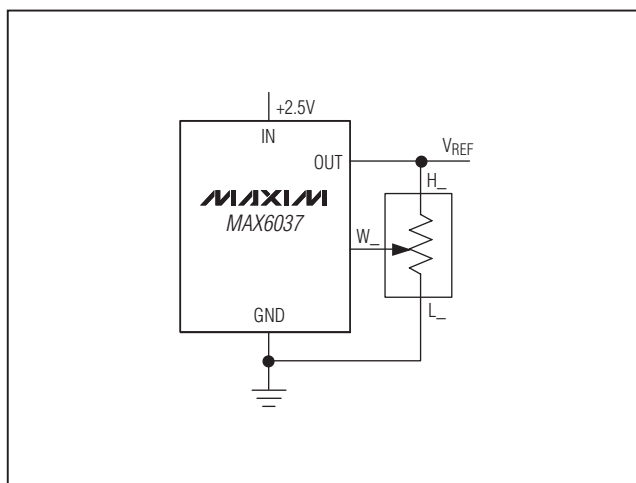


Figure 7. Adjustable Voltage Reference

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Variable-Gain Current-to-Voltage Converter

Figure 8 shows a variable-gain current-to-voltage converter using a potentiometer as a variable resistor.

## LCD Bias Control

Figure 9 shows a positive LCD bias control circuit using a potentiometer as a voltage-divider.

## Programmable Filter

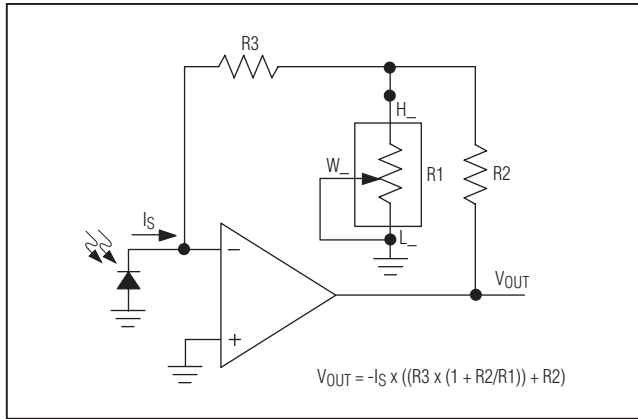
Figure 10 shows a programmable filter using a dual potentiometer.

## Offset Voltage Adjustment Circuit

Figure 11 shows an offset voltage adjustment circuit using a dual potentiometer.

## Process Information

PROCESS: BiCMOS



$$V_{OUT} = -I_S \times ((R_3 \times (1 + R_2/R_1)) + R_2)$$

Figure 8. Variable Gain I-to-V Converter

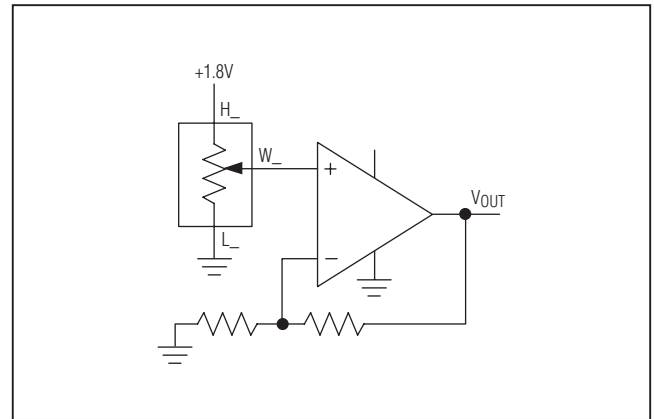


Figure 9. Positive LCD Bias Control Using a Voltage-Divider

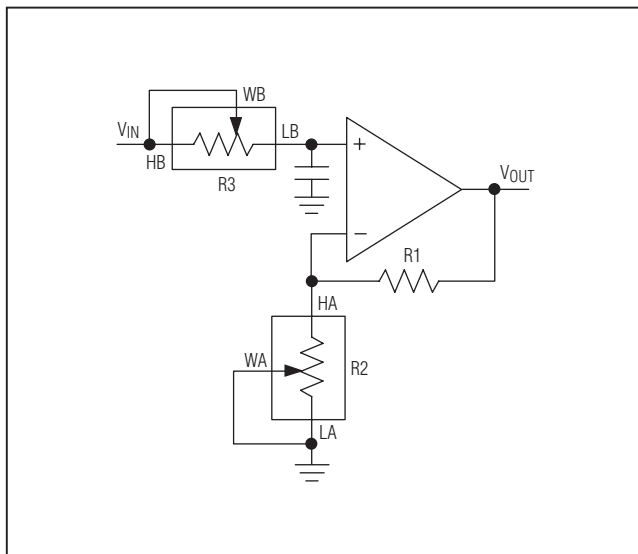


Figure 10. Programmable Filter

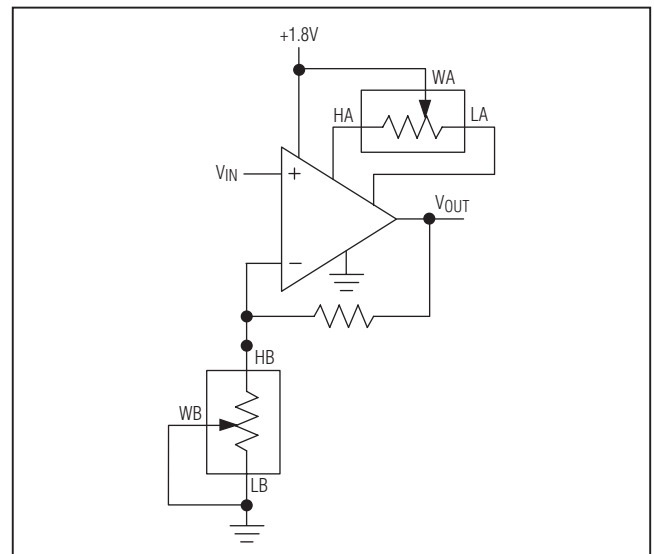


Figure 11. Offset Voltage Adjustment Circuit

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	<a href="#">21-0066</a>	<a href="#">90-0113</a>
16 TQFN-EP	T1633+5	<a href="#">21-0136</a>	<a href="#">90-0032</a>

MAX5391/MAX5393

# Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	4/10	Added Soldering Temperature in <i>Absolute Maximum Ratings</i> ; corrected code in Conditions of -3dB Bandwidth specification and corrected Integral Nonlinearity specifications in <i>Electrical Characteristics</i>	2
2	11/10	Changed <i>Electrical Characteristics</i> heading and changed Figures 5, 8, 10, 11	2, 3, 11, 12

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