

### Features

- Improved switch dV/dt immunity of 1500V/ $\mu$ s
- Drop-in replacement for CPC7592
- TTL logic level inputs for 3.3V logic interfaces
- Smart logic for power up / hot plug state control
- Small 16-pin SOIC Package
- Monolithic IC reliability
- Low matched  $R_{ON}$
- Eliminates the need for zero-cross switching
- Flexible switch timing to transition from ringing mode to talk mode
- Clean, bounce-free switching
- Tertiary protection consisting of integrated current limiting, voltage clamping, and thermal shutdown for SLIC protection
- 5V operation with power consumption <10mW
- Intelligent battery monitor
- Latched logic-level inputs, no external drive circuitry required

### Applications

- VoIP Gateways
- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks



### Description

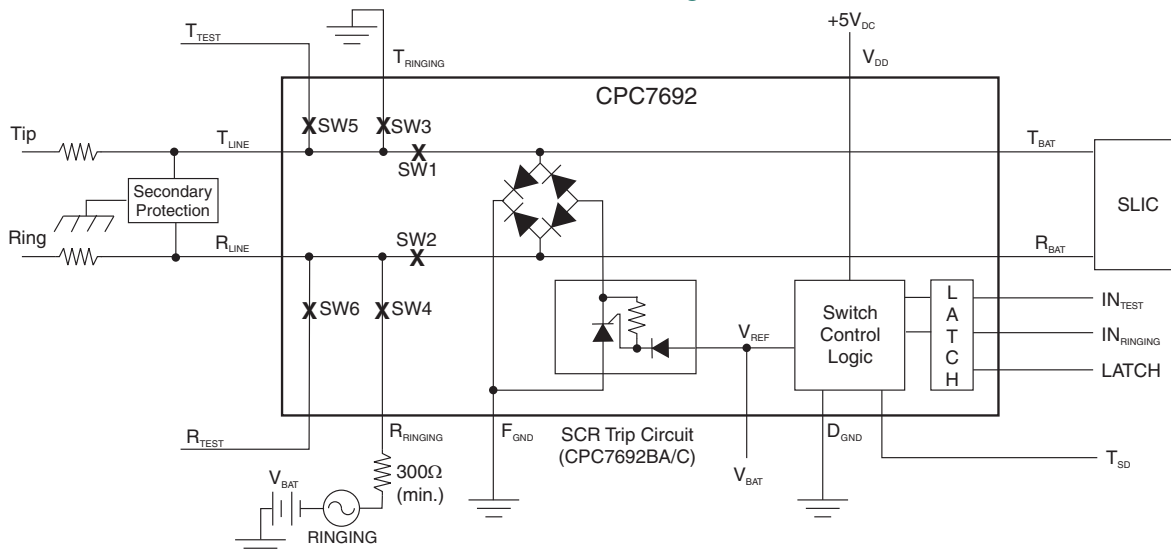
The CPC7692 is a member of IXYS IC Division's third-generation Line Card Access Switch (LCAS) family. Available in a 16-pin SOIC package, this monolithic 6-pole solid state switch provides the necessary functions to replace two 2-Form-C electromechanical relays used on traditional analog line cards and on contemporary integrated voice and data (IVD) line cards found in Central Office (CO), Access, and PBX equipment. This device contains solid state switches for tip and ring line break, ringing injection/return, and test access, requires only a +5V supply for operation and TTL logic-level inputs for control. The CPC7692 provides stable start-up conditioning during system power up, and for hot plug insertion applications. Once active, the inputs respond to traditional TTL logic levels, enabling the CPC7692 to be used with 3.3V logic devices.

The CPC7692BC has the same physical characteristics as the CPC7692BA but has an alternative logical set which provides different test states.

### Ordering Information

Device	Description
CPC7692BA	With Protection SCR, Tubes (50/Tube)
CPC7692BATR	With Protection SCR, Tape & Reel (1000/Reel)
CPC7692BB	Without Protection SCR, Tubes (50/Tube)
CPC7692BBTR	Without Protection SCR, Tape & Reel (1000/Reel)
CPC7692BC	With Protection SCR & "Alternate Logic States", Tubes (50/Tube)
CPC7692BCTR	With Protection SCR & "Alternate Logic States", Tape & Reel (1000/Reel)

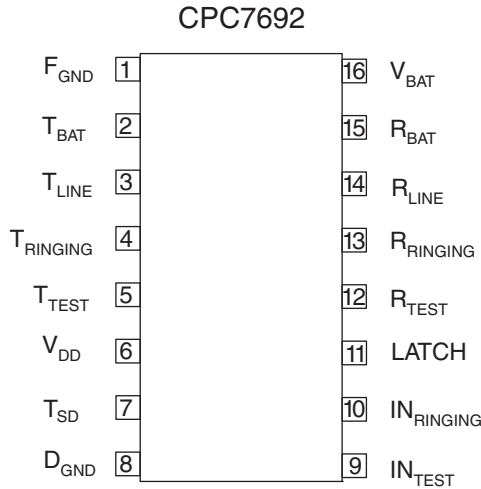
CPC7692 Block Diagram



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## 1. Specifications

### 1.1 Package Pinout



### 1.2 Pin Table

Pin	Name	Description
1	F <sub>GND</sub>	Fault ground
2	T <sub>BAT</sub>	Tip lead to the SLIC
3	T <sub>LINE</sub>	Tip lead of the line side
4	T <sub>RINGING</sub>	Ringing generator return
5	T <sub>TEST</sub>	Tip lead of the test bus
6	V <sub>DD</sub>	+5V supply
7	T <sub>SD</sub>	Temperature shutdown pin
8	D <sub>GND</sub>	Digital ground
9	IN <sub>TEST</sub>	Logic control input
10	IN <sub>RINGING</sub>	Logic control input
11	LATCH	Data latch enable control input
12	R <sub>TEST</sub>	Ring lead of the test bus
13	R <sub>RINGING</sub>	Ringing generator source
14	R <sub>LINE</sub>	Ring lead of the line side
15	R <sub>BAT</sub>	Ring lead to the SLIC
16	V <sub>BAT</sub>	Battery supply

### 1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
+5V power supply (V <sub>DD</sub> )	-0.3	7	V
Battery Supply	-	-85	V
D <sub>GND</sub> to F <sub>GND</sub> Separation	-5	+5	V
Logic input voltage	-0.3	V <sub>DD</sub> + 0.3	V
Logic input to switch output isolation	-	320	V
Switch open-contact isolation (SW1, SW2, SW3, SW5, SW6)	-	320	V
Switch open-contact Isolation (SW4)	-	465	V
Operating relative humidity	5	95	%
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

*Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.*

### 1.4 ESD Rating

ESD Rating (Human Body Model)
1000V

### 1.5 General Conditions

Unless otherwise specified, minimum and maximum values are production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the testing requirements.

Specifications cover the operating temperature range T<sub>A</sub> = -40° C to +85° C. Also, unless otherwise specified all testing is performed with V<sub>DD</sub> = 5V<sub>DC</sub>, logic low input voltage is 0V<sub>DC</sub> and logic high voltage is 5V<sub>DC</sub>.

### 1.6 Switch Specifications

#### 1.6.1 Break Switches, SW1 and SW2

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit	
Off-State Leakage Current	$V_{SW1}$ (differential) = $T_{LINE}$ to $T_{BAT}$ $V_{SW2}$ (differential) = $R_{LINE}$ to $R_{BAT}$ All-Off state.						
	+25° C, $V_{SW}$ (differential) = -320V to gnd $V_{SW}$ (differential) = +260V to -60V	$I_{SW}$	-	0.1	1	$\mu A$	
	+85° C, $V_{SW}$ (differential) = -330V to gnd $V_{SW}$ (differential) = +270V to -60V			0.3			
	-40° C, $V_{SW}$ (differential) = -310V to gnd $V_{SW}$ (differential) = +250V to -60V			0.1			
On Resistance	$I_{SW(on)}$ = $\pm 10$ mA, $\pm 40$ mA, $R_{BAT}$ and $T_{BAT}$ = -2V						
	+25° C	$R_{ON}$	-	14.5	-	$\Omega$	
	+85° C			20.5	28		
	-40° C			10.5	-		
On-Resistance Matching	Per SW1 & SW2 On-Resistance test conditions.	$\Delta R_{ON}$	-	0.15	0.8	$\Omega$	
Low Frequency Current Limit	$V_{SW}$ (on) = $\pm 10$ V, +25° C	$I_{SW}$	-	300	-	mA	
	$V_{SW}$ (on) = $\pm 10$ V, +85° C			80			160
	$V_{SW}$ (on) = $\pm 10$ V, -40° C			-			400
High Frequency Dynamic Current Limit ( $t \leq 0.5 \mu s$ )	Break switches on, all other switches off. Apply $\pm 1$ kV 10x1000 $\mu s$ pulse with appropriate protection in place.	$I_{SW}$	-	2.5	-	A	
Switch Outputs to Logic Input Isolation	+25° C, Logic inputs = gnd, $V_{SW}$ ( $T_{LINE}$ , $R_{LINE}$ ) = $\pm 320$ V	$I_{SW}$	-	0.1	1	$\mu A$	
	+85° C, Logic inputs = gnd, $V_{SW}$ ( $T_{LINE}$ , $R_{LINE}$ ) = $\pm 330$ V			-			0.3
	-40° C, Logic inputs = gnd, $V_{SW}$ ( $T_{LINE}$ , $R_{LINE}$ ) = $\pm 310$ V			-			0.1
Transient Immunity	100V <sub>PP</sub> Square Wave, 100Hz (Not production tested - limits are guaranteed by design and quality control sampling audits.)	dV/dt	1500	2100	-	V/ $\mu s$	

1.6.2 Ringing Return Switch, SW3

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	$V_{SW3}$ (differential) = $T_{LINE}$ to $T_{RINGING}$ All-Off state.					
	+25° C, $V_{SW}$ (differential) = -320V to gnd $V_{SW}$ (differential) = +260V to -60V	$I_{SW}$	-	0.1	1	$\mu A$
	+85° C, $V_{SW}$ (differential) = -330V to gnd $V_{SW}$ (differential) = +270V to -60V			0.3		
-40° C, $V_{SW}$ (differential) = -310V to gnd $V_{SW}$ (differential) = +250V to -60V	0.1					
On Resistance	$I_{SW}(on)$ = $\pm 0$ mA, $\pm 10$ mA, +25° C	$R_{ON}$	-	60	-	$\Omega$
	$I_{SW}(on)$ = $\pm 0$ mA, $\pm 10$ mA, +85° C			85	100	
	$I_{SW}(on)$ = $\pm 0$ mA, $\pm 10$ mA, -40° C			45	-	
Low Frequency Current Limit	$V_{SW}$ (on) = $\pm 10$ V, +25° C	$I_{SW}$	-	135	-	mA
	$V_{SW}$ (on) = $\pm 10$ V, +85° C		70	85		
	$V_{SW}$ (on) = $\pm 10$ V, -40° C		-	210		
High Frequency Dynamic Current Limit ( $t \leq 0.5 \mu s$ )	Ringing switches on, all other switches off. Apply $\pm 1kV$ $10 \times 1000 \mu s$ pulse with appropriate protection in place.	$I_{SW}$	-	2.5	-	A
Switch Outputs to Logic Input Isolation	+25° C, Logic inputs = gnd, $V_{SW}$ ( $T_{RINGING}$ , $T_{LINE}$ ) = $\pm 320$ V	$I_{SW}$	-	0.1	1	$\mu A$
	+85° C, Logic inputs = gnd, $V_{SW}$ ( $T_{RINGING}$ , $T_{LINE}$ ) = $\pm 330$ V			0.3		
	-40° C, Logic inputs = gnd, $V_{SW}$ ( $T_{RINGING}$ , $T_{LINE}$ ) = $\pm 310$ V			0.1		
Transient Immunity	100V <sub>pp</sub> Square Wave, 100Hz (Not production tested - limits are guaranteed by design and quality control sampling audits.)	dV/dt	1500	2100	-	V/ $\mu s$

1.6.3 Ringing Switch, SW4

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	$V_{SW4}$ (differential) = $R_{LINE}$ to $R_{RINGING}$ All-Off state.					
	+25° C $V_{SW}$ (differential) = -255V to +210V $V_{SW}$ (differential) = +255V to -210V	$I_{SW}$	-	0.05	1	$\mu A$
	+85° C $V_{SW}$ (differential) = -270V to +210V $V_{SW}$ (differential) = +270V to -210V			0.1		
	-40° C $V_{SW}$ (differential) = -245V to +210V $V_{SW}$ (differential) = +245V to -210V			0.05		
On Resistance	$I_{SW}$ (on) = $\pm 70$ mA, $\pm 80$ mA	$R_{ON}$	-	10	15	$\Omega$
On Voltage	$I_{SW}$ (on) = $\pm 1$ mA	$V_{ON}$	-	1.5	3	V
On-State Leakage Current	Inputs set for ringing -Measure ringing generator current to ground.	$I_{RINGING}$	-	0.1	0.25	mA
Steady-State Current*	Inputs set for ringing mode.	$I_{SW}$	-	-	150	mA
Surge Current*	Ringing switches on, all other switches off. Apply $\pm 1kV$ $10 \times 1000 \mu s$ pulse with appropriate protection in place.	$I_{SW}$	-	-	2	A
Release Current	SW4 transition from on to off.	$I_{RINGING}$	-	300	-	$\mu A$
Switch Outputs to Logic Input Isolation	+25° C, Logic inputs = gnd, $V_{SW}$ ( $R_{RINGING}$ , $R_{LINE}$ ) = $\pm 320V$	$I_{SW}$	-	0.1	1	$\mu A$
	+85° C, Logic inputs = gnd, $V_{SW}$ ( $R_{RINGING}$ , $R_{LINE}$ ) = $\pm 330V$			0.3		
	-40° C, Logic inputs = gnd, $V_{SW}$ ( $R_{RINGING}$ , $R_{LINE}$ ) = $\pm 310V$			0.1		
Transient Immunity	100V <sub>PP</sub> Square Wave, 100Hz (Not production tested - limits are guaranteed by design and quality control sampling audits.)	dV/dt	1500	2100	-	V/ $\mu s$

\*Secondary protection and current limiting must prevent exceeding this parameter.

1.6.4 Test Switches, SW5 and SW6

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit	
Off-State Leakage Current	$V_{SW1}$ (differential) = $T_{LINE}$ to $T_{BAT}$ $V_{SW2}$ (differential) = $R_{LINE}$ to $R_{BAT}$ All-Off state.						
	+25° C, $V_{SW}$ (differential) = -320V to gnd $V_{SW}$ (differential) = +260V to -60V	$I_{SW}$	-	0.1	1	$\mu A$	
	+85° C, $V_{SW}$ (differential) = -330V to gnd $V_{SW}$ (differential) = +270V to -60V			0.3			
	-40° C, $V_{SW}$ (differential) = -310V to gnd $V_{SW}$ (differential) = +250V to -60V			0.1			
On Resistance	$I_{SW}(on) = \pm 10$ mA, $\pm 40$ mA, $R_{BAT}$ and $T_{BAT} = -2$ V						
	+25° C	$R_{ON}$	-	38	-	$\Omega$	
	+85° C			46	70		
	-40° C			28	-		
Low Frequency Current Limit	$V_{SW}$ (on) = $\pm 10$ V, +25° C	$I_{SW}$	-	175	-	mA	
	$V_{SW}$ (on) = $\pm 10$ V, +85° C			80			110
	$V_{SW}$ (on) = $\pm 10$ V, -40° C			-			210
High Frequency Dynamic Current Limit ( $t \leq 0.5 \mu s$ )	Break switches on, all other switches off. Apply $\pm 1$ kV 10x1000 $\mu s$ pulse with appropriate protection in place.	$I_{SW}$	-	2.5	-	A	
Switch Outputs to Logic Input Isolation	+25° C, Logic inputs = gnd, $V_{SW}$ ( $T_{LINE}$ , $R_{LINE}$ ) = $\pm 320$ V	$I_{SW}$	-	0.1	1	$\mu A$	
	+85° C, Logic inputs = gnd, $V_{SW}$ ( $T_{LINE}$ , $R_{LINE}$ ) = $\pm 330$ V			0.3			
	-40° C, Logic inputs = gnd, $V_{SW}$ ( $T_{LINE}$ , $R_{LINE}$ ) = $\pm 310$ V			0.1			
Transient Immunity	100V <sub>PP</sub> Square Wave, 100Hz (Not production tested - limits are guaranteed by design and quality control sampling audits.)	dV/dt	1500	2100	-	V/ $\mu s$	

1.7 Digital I/O Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
<b>Input Voltage Thresholds</b>						
Logic Low	Input voltage falling	$V_{IL}$	0.8	1.1	-	V
Logic High	Input voltage rising	$V_{IH}$		1.7	2.0	
<b>Input Leakage Current</b>						
Logic High	$V_{DD} = 5.5V, V_{BAT} = -75V, V_{IH} = 2.4V$	$I_{IH}$				$\mu A$
$I_{NRINGING}$ and $I_{NTEST}$			-	0.1	1	
LATCH			10	28	-	
$T_{SD}$			10	16	30	
Logic Low	$V_{DD} = 5.5V, V_{BAT} = -75V, V_{IL} = 0.4V$	$I_{IL}$				$\mu A$
$I_{NRINGING}$ and $I_{NTEST}$			-	0.1	1	
LATCH			-	46	125	
$T_{SD}$			10	16	30	
<b><math>T_{SD}</math> Output Voltage Levels</b>						
Logic High	$V_{DD} = 5.5V, V_{BAT} = -75V, I_{TSD} = 10\mu A$	$V_{TSD\_off}$	2.4	$V_{DD}$	-	V
Logic Low	$V_{DD} = 5.5V, V_{BAT} = -75V, I_{TSD} = 1mA$	$V_{TSD\_on}$	-	0	0.4	V

1.8 Voltage and Power Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
<b>Voltage Requirements</b>						
$V_{DD}$	-	$V_{DD}$	4.5	5.0	5.5	V
$V_{BAT}^1$	-	$V_{BAT}$	-19	-48	-72	V
<small><sup>1</sup><math>V_{BAT}</math> is used only for internal protection circuitry. If <math>V_{BAT}</math> rises above -10V, the device will enter the all-off state and will remain in the all-off state until the battery drops below approximately -15V</small>						
<b>Power Specifications</b>						
Power Consumption	$V_{DD} = 5V, V_{BAT} = -48V, V_{IH} = 2.4V, V_{IL} = 0.4V, \text{Measure } I_{DD} \text{ and } I_{BAT}$	P				mW
Talk and All-Off States			-	5.5	10	
All Other States				6.5	10	
$V_{DD}$ Current	$V_{DD} = 5V, V_{BAT} = -48V, V_{IH} = 2.4V, V_{IL} = 0.4V$	$I_{DD}$				mA
Talk and All-Off States			-	1.1	2.0	
Ringing State				1.3	2.0	
$V_{BAT}$ Current - Any State	$V_{DD} = 5V, V_{BAT} = -48V, V_{IH} = 2.4V, V_{IL} = 0.4V$	$I_{BAT}$	-	0.1	10	$\mu A$



1.9 Protection Circuitry Electrical Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
<b>Protection Diode Bridge</b>						
Forward Voltage Drop, Continuous Current (50/60 Hz)	Apply ± DC current limit of break switches	$V_F$	-	2.1	3.0	V
Forward Voltage Drop, Surge Current	Apply ± dynamic current limit of break switches	$V_F$	-	5	-	
<b>Protection SCR (CPC7692BA and CPC7692BC)</b>						
Surge current	-	-	-	-	*	A
Trigger Current: Current into $V_{BAT}$ Pin.	SCR activates, +25° C	$I_{TRIG}$	-	70	-	mA
	SCR activates, +85° C			40		
Hold Current: Current Through Protection SCR	SCR remains active, +25° C	$I_{HOLD}$	-	135	-	mA
	SCR remains active, +85° C			110		
Gate Trigger Voltage	$I_{GATE} = I_{TRIGGER}^{\S}$	$V_{TBAT}$ or $V_{RBAT}$	$V_{BAT} - 4$	-	$V_{BAT} - 2$	V
Reverse Leakage Current	$V_{BAT} = -48V$	$I_{VBAT}$	-	-	1.0	μA
On-State Voltage	0.5 A, t = 0.5 μs	$V_{TBAT}$ or $V_{RBAT}$	-	-3	-	V
	2.0 A, t = 0.5 μs			-5		
<b>Temperature Shutdown Specifications</b>						
Shutdown Activation Temperature	Not production tested - limits are guaranteed by design and Quality Control sampling audits.	$T_{TSD\_on}$	110	125	150	°C
Shutdown Circuit Hysteresis		$T_{TSD\_off}$	10	-	25	°C
*Passes GR1089 and ITU-T K.20 with appropriate secondary protection in place.						
<sup>§</sup> $V_{BAT}$ must be capable of sourcing $I_{TRIGGER}$ for the internal SCR to activate.						

1.10 Truth Tables

1.10.1 CPC7692BA and CPC7692BB Truth Table

State	INRINGING	INTEST	LATCH	TSD	Break Switches	Ringing Switches	Test Switches
Talk	0	0	0	Z <sup>1</sup>	On	Off	Off
Test	0	1			Off	Off	On
Ringing	1	0			Off	On	Off
All-Off	1	1			Off	Off	Off
Latched	X	X	1	0	Unchanged		
All-Off	X	X	X		Off	Off	Off

<sup>1</sup> Z = High Impedance. Because TSD has an internal pull up at this pin, it should be controlled with an open-collector or open-drain type device.

1.10.2 CPC7692BC Truth Table

State	INRINGING	INTEST	LATCH	TSD	Break Switches	Ringing Switches	Test Switches
Talk	0	0	0	Z <sup>1</sup>	On	Off	Off
Test/Monitor	0	1			On	Off	On
Ringing	1	0			Off	On	Off
Ringing Test	1	1			Off	On	On
Latched	X	X	1	0	Unchanged		
All-Off	X	X	X		Off	Off	Off

<sup>1</sup> Z = High Impedance. Because TSD has an internal pull up at this pin, it should be controlled with an open-collector or open-drain type device.

## 2. Functional Description

### 2.1 Introduction

#### 2.1.1 CPC7692BA and CPC7692BB Logic States

- **Talk.** Break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.
- **Ringing.** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 closed, and test switches SW5 and SW6 open.
- **Test.** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and loop test switches SW5 and SW6 closed.
- **All-off.** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.

#### 2.1.2 CPC7692BC Logic States

- **Talk.** Break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.
- **Ringing.** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 closed, and test switches SW5 and SW6 open.
- **Test/Monitor.** Break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 closed.
- **Ringing Test.** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 closed, and test switches SW5 and SW6 closed.
- **All-off.** Break switches SW1 and SW2 open, ringing switches SW3 and SW4 open, and test switches SW5 and SW6 open.

The CPC7692 offers break-before-make and make-before-break switching from the ringing state to the talk state with simple TTL level logic input control. Solid-state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, eliminating the need for external zero-cross switching circuitry. State control is via TTL logic-level input so no additional driver circuitry is required. The linear break switches SW1 and SW2 have exceptionally low  $R_{ON}$  and excellent matching characteristics. The ringing switch, SW4, has a minimum open contact breakdown voltage of 465V at +25°C sufficiently high with proper protection to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Integrated into the CPC7692 is an over-voltage clamping circuit, active current limiting, and a thermal shutdown mechanism to provide protection for the SLIC during a fault condition. Positive and negative lightning surge currents are reduced by the current limiting circuitry and hazardous potentials are diverted away from the SLIC via the protection diode bridge or the optional integrated protection SCR. Power-cross potentials are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC7692 from an over-voltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the  $T_{LINE}$  and  $R_{LINE}$  terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is highly recommended. With proper selection of the secondary protector, a line card using the CPC7692 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

The CPC7692 operates from a single +5V supply. This gives the device extremely low power consumption in any state with virtually any range of battery voltage. The battery voltage used by the CPC7692 has a two fold function. During surge conditions the internal integrated protection circuitry uses the battery voltage as a reference and as a current source. Second, the battery voltage is used as a reference. In the event of battery voltage loss, the CPC7692 will enter the all-off state.

### 2.2 Under Voltage Switch Lock Out Circuitry

#### 2.2.1 Introduction

Smart logic in the CPC7692 now provides for switch state control during both power up and power loss transitions. An internal detector is used to evaluate the  $V_{DD}$  supply to determine when to de-assert the under voltage switch lock out circuitry with a rising  $V_{DD}$  and when to assert the under voltage switch lock out circuitry with a falling  $V_{DD}$ . Any time unsatisfactory low  $V_{DD}$  conditions exist the lock out circuit overrides user switch control by blocking the information at the external input pins and conditioning internal switch

commands to the all off state. Upon restoration of  $V_{DD}$  the switches will remain in the all-off state until the LATCH input is pulled low.

The rising  $V_{DD}$  lock out release threshold is internally set to ensure all internal logic is properly biased and functional before accepting external switch commands from the inputs to control the switch states. For a falling  $V_{DD}$  event, the lock out threshold is set to assure proper logic and switch behavior up to the moment the switches are forced off and external inputs are suppressed.

To facilitate hot plug insertion and power up control the LATCH pin has an integrated weak pull up resistor to the  $V_{DD}$  power rail that will hold a non-driven LATCH pin at a logic high state. This enables board designers to use the CPC7692 with FPGAs and other devices that provide high impedance outputs during power up and configuration. The weak pull up allows a fan out of up to 32 when the system's LATCH control driver has a logic low minimum sink capability of 4mA.

#### 2.2.2 Hot Plug and Power Up Circuit Design Considerations

There are six possible start up scenarios that can occur during power up. They are:

1. All inputs defined at power up & LATCH = 0
2. All inputs defined at power up & LATCH = 1
3. All inputs defined at power up & LATCH = Z
4. All inputs not defined at power up & LATCH = 0
5. All inputs not defined at power up & LATCH = 1
6. All inputs not defined at power up & LATCH = Z

Under all of the start up situations listed above the CPC7692 will hold all of it's switches in the all-off state during power up. When  $V_{DD}$  requirements have been satisfied the LCAS will complete it's start up procedure in one of three conditions.

For start up scenario 1 the CPC7692 will transition from the all off state to the state defined by the inputs when  $V_{DD}$  is valid.

For start up scenarios 2, 3, 5, and 6 the CPC7692 will power up in the all-off state and remain there until the LATCH pin is pulled low. This allows for an indefinite all off state for boards inserted into a powered system but are not configured for service or boards that need to wait for other devices to be configured first.

Start up scenario 4 will start up with all switches in the all-off state but upon the acceptance of a valid  $V_{DD}$  the LCAS will revert to one of the legitimate states listed in the truth tables and there after may randomly change states based on input pin leakage currents and loading. Because the LCAS state after power up can not be predicted with this start up condition it should never be utilized.

On designs that do not wish to individually control the LATCH pins of multi-port cards it is possible to bus many (or all) of the LATCH pins together to create a single board level input enable control.

### 2.3 Switch Logic

#### 2.3.1 Start-up

The CPC7692 uses smart logic to monitor the  $V_{DD}$  supply. Any time the  $V_{DD}$  is below an internally set threshold, the smart logic places the Switch Control Logic into the all-off state. An internal pullup at the LATCH pin locks the CPC7692 in the all-off state following start-up until the LATCH pin is pulled down to a logic low. Prior to the assertion of a logic low at the LATCH pin, the switch control inputs must be properly conditioned.

#### 2.3.2 Switch Timing

The CPC7692 provides, when switching from the ringing state to the talk state, the ability to control the release timing of the ringing switches SW3 and SW4 relative to the state of the switches SW1 and SW2 using simple TTL logic-level inputs. The two available techniques are referred to as make-before-break and break-before-make operation. When the break switch contacts of SW1 and SW2 are closed (made) before the ringing switch contacts of SW3 and SW4 are opened (broken), this is referred to as make-before-break operation. Break-before-make operation occurs when the ringing contacts of SW3 and SW4 are opened (broken) before the switch contacts of SW1 and SW2 are closed (made). With the CPC7692, make-before-break and break-before-make operations can easily be accomplished by applying the proper sequence of logic-level inputs to the device.

The logic sequences for either mode of operation are provided in **“Ringing to Talk Transition Logic Sequence for All Versions: Make-Before-Break” on page 13**, **“Ringing to Talk Transition Logic**

Sequence CPC7692BA/B: Break-Before-Make” on page 13, and “Ringing to Talk Transition Logic Sequence for all Versions: Break-Before-Make” on page 14. Logic states and input control settings are provided in “CPC7692BA and CPC7692BB Truth Table” on page 10 and “CPC7692BC Truth Table” on page 10.

state. Application of the talk state opens the ringing return switch, SW3, as the break switches SW1 and SW2 close. The ringing switch, SW4, remains closed until the next zero-crossing of the ringing current. While in the make-before-break state, ringing potentials in excess of the CPC7692 protection circuitry thresholds will be diverted away from the SLIC.

2.3.3 Make-Before-Break Operation - All Versions

To use the make-before-break operation, change the logic inputs from the ringing state directly to the talk

Ringing to Talk Transition Logic Sequence for All Versions: Make-Before-Break

State	IN <sub>RINGING</sub>	IN <sub>TEST</sub>	LATCH	T <sub>SD</sub>	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	0	Z	-	Off	On	On	Off
Make-Before-Break	0	0			SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of the ringing cycle. In this transition state current limited by the DC break switch current limit value will be sourced from the ring node of the SLIC.	On	Off	On	Off
Talk	0	0			Zero-cross current has occurred	On	Off	Off	Off

2.3.4 Break-Before-Make Operation - CPC7692BA/B

Break-before-make operation of the CPC7692BA/B can be achieved using two different techniques.

The first method uses manipulation of the IN<sub>RINGING</sub> and IN<sub>TEST</sub> logic inputs as shown in “Ringing to Talk Transition Logic Sequence CPC7692BA/B: Break-Before-Make” on page 13.

remains on, waiting for the next zero current event.

- Hold the all off state for at least one-half of a ringing cycle to assure that a zero crossing event occurs allowing SW4, the ringing switch, to open.
- Apply inputs for the next desired state. For the talk state, the inputs would be (0,0).

- At the end of the ringing state apply the all off state (1,1). This releases the ringing return switch (SW3) while the ringing switch (SW4)

Break-before-make operation occurs when the ringing switches open before the break switches SW1 and SW2 close.

Ringing to Talk Transition Logic Sequence CPC7692BA/B: Break-Before-Make

State	IN <sub>RINGING</sub>	IN <sub>TEST</sub>	LATCH	T <sub>SD</sub>	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	0	Z	-	Off	On	On	Off
All-Off	1	1			Hold this state for at least one-half of the ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On	Off
Break-Before-Make	1	1			Zero current has occurred. SW4 has opened	Off	Off	Off	Off
Talk	0	0			Break switches close.	On	Off	Off	Off

2.3.5 Break-Before-Make Operation - All Versions

The second break-before-make method for the CPC7692BA/B is also the only method available for the CPC7692BC. As shown in “CPC7692BA and CPC7692BB Truth Table” on page 10 and “CPC7692BC Truth Table” on page 10, the bidirectional T<sub>SD</sub> interface disables all of the CPC7692 switches when pulled to a logic low. Although logically disabled, an active (closed) ringing switch (SW4) will remain closed until the next zero crossing current event.

As shown in the table “Ringing to Talk Transition Logic Sequence for all Versions: Break-Before-Make” on page 14, this operation is similar to the one shown in “Ringing to Talk Transition Logic Sequence CPC7692BA/B: Break-Before-Make” on page 13, except in the method used to select the all off state, and in when the IN<sub>RINGING</sub> and IN<sub>TEST</sub> inputs are configured for the talk state.

1. Pull T<sub>SD</sub> to a logic low to end the ringing state. This opens the ringing return switch (SW3) and prevents any other switches from closing.
2. Keep T<sub>SD</sub> low for at least one-half the duration of the ringing cycle period to allow sufficient time for a zero crossing current event to occur and for the circuit to enter the break-before-make state.
3. During the T<sub>SD</sub> low period, set the IN<sub>RINGING</sub> and IN<sub>TEST</sub> inputs to the talk state (0, 0).
4. Release T<sub>SD</sub>, allowing the internal pull-up to activate the break switches.

When using T<sub>SD</sub> as an input, the two recommended states are “0” which overrides the logic input pins and forces an all off state and “Z” which allows normal switch control via the logic input pins. This requires the use of an open-collector or open-drain type buffer.

Ringing to Talk Transition Logic Sequence for all Versions: Break-Before-Make

State	IN <sub>RINGING</sub>	IN <sub>TEST</sub>	LATCH	T <sub>SD</sub>	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)	Test Switches
Ringing	1	0	0	Z	-	Off	On	On	Off
All-Off	1	0	X	0	Hold this state for at least one-half of the ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On	Off
Break-Before-Make	0	0			SW4 has opened	Off	Off	Off	Off
Talk	0	0	0	Z	Close Break Switches	On	Off	Off	Off

2.4 Data Latch

The CPC7692 has an integrated transparent data latch. The latch enable operation is controlled by TTL logic input levels at the LATCH pin. Data input to the latch is via the input pins IN<sub>RINGING</sub> and IN<sub>TEST</sub> while the output of the data latch are internal nodes used for state control. When the LATCH enable control pin is at a logic 0 the data latch is transparent and the input control signals flow directly through the data latch to the state control circuitry. A change in input will be reflected by a change in the switch state.

Whenever the LATCH enable control pin is at logic 1, the data latch is active and data is locked. Subsequent

changes to the input controls IN<sub>RINGING</sub> and IN<sub>TEST</sub> will not result in a change to the control logic or affect the existing switch state.

The switches will remain in the state they were in when the LATCH changes from logic 0 to logic 1 and will not respond to changes in input as long as the LATCH is at logic 1. However, neither the T<sub>SD</sub> input nor the T<sub>SD</sub> output control functions are affected by the latch function. Since internal thermal shutdown control and external “All-off” control is not affected by the state of the LATCH enable input, T<sub>SD</sub> will override state control.

## 2.5 T<sub>SD</sub> Pin Description

The T<sub>SD</sub> pin is a bidirectional I/O structure with an internal pull-up current source having a nominal value of 16  $\mu$ A biased from V<sub>DD</sub>. As an output, this pin indicates the status of the thermal shutdown circuitry. During normal operation, this pin will typically be pulled up to V<sub>DD</sub> but under fault conditions that create excess thermal loading the CPC7692 will enter thermal shutdown and a logic low will be output.

As an input, the T<sub>SD</sub> pin is utilized to place the CPC7692 into the “All-Off” state by simply pulling the input low. For applications using low-voltage logic devices (lower than V<sub>DD</sub>), IXYS IC Division recommends the use of an open-collector or an open-drain type output to control T<sub>SD</sub>. This avoids sinking the T<sub>SD</sub> pull up bias current to ground during normal operation when the all-off state is not required. In general, IXYS IC Division recommends all applications use an open-collector or open-drain type device to drive this pin.

Driving the T<sub>SD</sub> input to a logic high or tying it to V<sub>DD</sub> will not override the thermal shutdown mechanism.

## 2.6 Ringing Switch Zero-Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ringing switch is designed to delay the change in state until the next zero-crossing. Once on, the switch requires a zero-current cross to turn off, and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter the logic input until the next zero crossing. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing switches. See IXYS IC Division’s application note AN-144, **Impulse Noise Benefits of Line Card Access Switches** for more information. The attributes of ringing switch SW4 may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300  $\Omega$  in series with the ringing generator is recommended.

## 2.7 Power Supplies

Both a +5V supply and battery voltage are connected to the CPC7692. Switch state control is powered exclusively by the +5V supply. As a result, the CPC7692 exhibits extremely low power consumption during active and idle states.

Although battery power is not used for switch control, it is required to supply trigger current for the integrated internal protection circuitry SCR during fault conditions. This integrated SCR is designed to activate whenever the voltage at T<sub>BAT</sub> or R<sub>BAT</sub> drops 2 to 4 V below the applied voltage on the V<sub>BAT</sub> pin. Because the battery supply at this pin is required to source trigger current during negative overvoltage fault conditions at tip and ring, it is important that the net supplying this current be a low impedance path for high speed transients such as lightning. This will permit trigger currents to flow enabling the SCR to activate and thereby prevent a fault induced negative overvoltage event at the T<sub>BAT</sub> or R<sub>BAT</sub> nodes.

## 2.8 Battery Voltage Monitor

The CPC7692 also uses the V<sub>BAT</sub> voltage to monitor battery voltage. If system battery voltage is lost, the CPC7692 immediately enters the all-off state. It remains in this state until the battery voltage is restored. The device also enters the all-off state if the battery voltage rises more positive than about –10V with respect to ground and remains in the all-off state until the battery voltage drops below approximately –15 V with respect to ground. This battery monitor feature draws a small current from the battery (less than 1  $\mu$ A typical) and will add slightly to the device’s overall power dissipation.

This monitor function performs properly if the CPC7692 and SLIC share a common battery supply origin. Otherwise, if battery is lost to the CPC7692 but not to the SLIC, then the V<sub>BAT</sub> pin will be internally biased by the potential applied at the T<sub>BAT</sub> or R<sub>BAT</sub> pins via the internal protection circuitry SCR trigger current path.

## 2.9 Protection

### 2.9.1 Diode Bridge/SCR

The CPC7692 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground via F<sub>GND</sub>. Voltage is clamped to a diode drop above ground. During a negative transient of 2 to 4V more

negative than the voltage source at  $V_{BAT}$ , the SCR conducts and faults are shunted to  $F_{GND}$  via the SCR or the diode bridge.

In order for the SCR to crowbar (or foldback), the SCR's on-voltage (see "**Protection Circuitry Electrical Specifications**" on page 9) must be less than the applied voltage at the  $V_{BAT}$  pin. If the  $V_{BAT}$  voltage is less negative than the SCR on-voltage or if the  $V_{BAT}$  supply is unable to source the trigger current, the SCR will not crowbar.

For power induction or power-cross fault conditions, the positive cycle of the transient is clamped to a diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the  $V_{BAT}$  reference voltage by two to four volts, steering the fault current to ground.

Note: The CPC7692BB does not contain the protection SCR but instead uses diodes to clamp both polarities of a transient fault. These diodes direct the negative potential's fault current to the  $V_{BAT}$  pin.

### 2.9.2 Current Limiting function

If a lightning strike transient occurs when the device is in the talk state, the current is passed along the line to the integrated protection circuitry and restricted by the High Frequency Dynamic Current Limit response of the active switches. During the talk state, when a 1000V 10x1000  $\mu$ s lightning pulse (GR-1089-CORE) is applied to the line through a properly clamped external protector, the current seen at  $T_{LINE}$  and  $R_{LINE}$  will be a pulse with a typical magnitude of 2.5 A and a duration less than 0.5  $\mu$ s.

If a power-cross fault occurs with the device in the talk state, the current passes through the break switches SW1 and SW2 to the integrated protection circuit but is limited by the Low Frequency Current Limit response of the two break switches. The Low Frequency Current Limit specified over temperature is between 80 mA and 425 mA with the circuitry having a negative temperature coefficient. As a result, if the device is subjected to extended heating due to a power cross fault condition, the measured current at  $T_{LINE}$  and  $R_{LINE}$  will decrease as the device temperature increases. If the device temperature rises sufficiently, the thermal shutdown mechanism will activate and the device will enter the all-off state.

### 2.10 Thermal Shutdown

The thermal shutdown mechanism activates when the device die temperature reaches a minimum of 110° C, placing the device in the all-off state regardless of logic input. During thermal shutdown events the  $T_{SD}$  pin will output a logic low with a nominal 0V level. A logic high is output from the  $T_{SD}$  pin during normal operation with a typical output level equal to  $V_{DD}$ . As stated earlier, the thermal shutdown feature can not be disabled by forcing a logic high to the  $T_{SD}$  input.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross event, the device temperature will rise and the thermal shutdown mechanism will activate forcing the switches to the all-off state. At this point the current measured into  $T_{LINE}$  or  $R_{LINE}$  will drop to zero. Once the device enters thermal shutdown it will remain in the all-off state until the temperature of the device drops below the de-activation level of the thermal shutdown circuit. This permits the device to autonomously return to normal operation. If the fault has not passed, current will again flow up to the value allowed by the current limiting of the switches and heating will resume, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector will activate shunting the fault current to ground.

### 2.11 External Protection Elements

The CPC7692 requires only over voltage secondary protection on the loop side of the device. The integrated protection feature described above negates the need for additional external protection on the SLIC side. The secondary protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7692. A foldback or crowbar type protector is recommended to minimize stresses on the CPC7692.

Consult IXYS IC Division's application note, AN-100, **Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces** for equations related to the specifications of external secondary protectors, fused resistors and PTCs.



### 3. Manufacturing Information

#### 3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC7692BA / CPC7692BB / CPC7692BC	MSL 1

#### 3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

#### 3.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC7692BA / CPC7692BB / CPC7692BC	260°C for 30 seconds

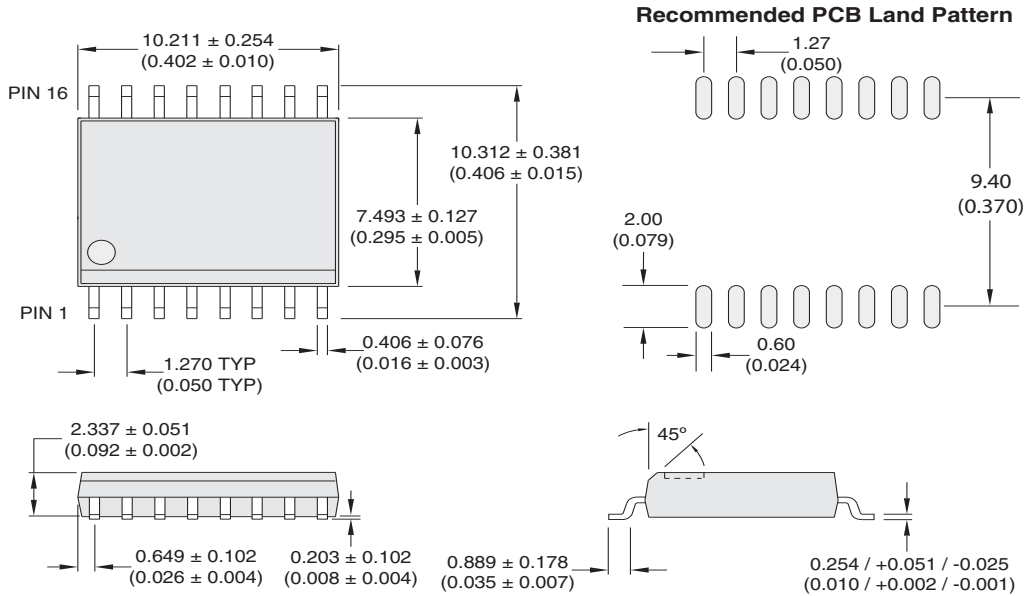
#### 3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.



### 3.5 Mechanical Dimensions

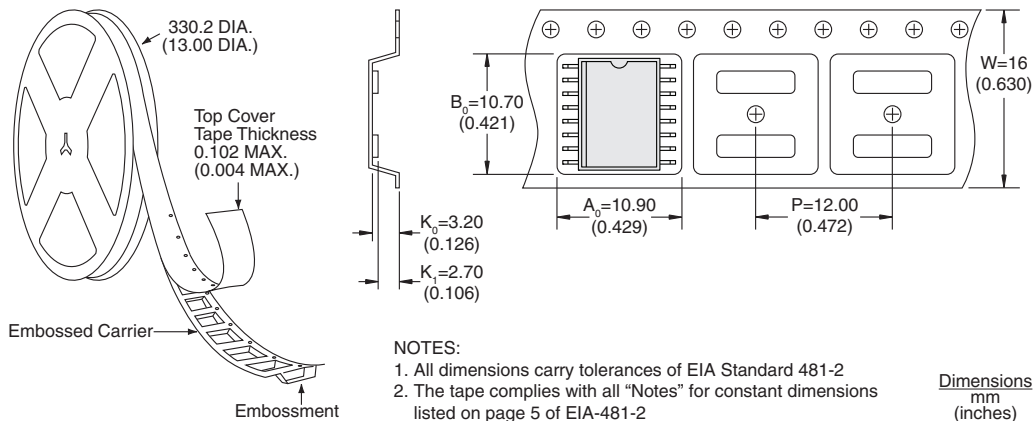
#### 3.5.1 CPC7692Bx 16-Pin SOIC Package



- NOTES:  
 1. Coplanarity = 0.1016 (0.004) max.  
 2. Leadframe thickness does not include solder plating (1000 microinch maximum).

**DIMENSIONS**  
 mm  
 (inches)

#### 3.5.2 CPC7692BxTR Tape & Reel



- NOTES:  
 1. All dimensions carry tolerances of EIA Standard 481-2  
 2. The tape complies with all "Notes" for constant dimensions listed on page 5 of EIA-481-2

**Dimensions**  
 mm  
 (inches)

For additional information please visit [www.ixysic.com](http://www.ixysic.com)

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